Reg. No.										

प्रज्ञानं ब्रह्म

Manipal

INSPIRED BY LIFE

INTERNATIONAL CENTRE FOR APPLIED SCIENCES

(Manipal University)

III SEMESTER B.S. DEGREE EXAMINATION – MAY 2016

SUBJECT: COMBINATIINAL AND SEQUENTIAL LOGIC (EC 231)

(BRANCH: COMP SCIENCE/COMP ENGG/E&C/E&E)

26TH MAY, 2016

Time: 3 Hours **Max. Marks: 100**

- ✓ **Answer ANY FIVE full Questions.**

1A. Solve the following:

i. Convert $(9786.3247)_{10}$ to hexadecimal.
ii. Convert $(324.213)_5$ to decimal number.
iii. Convert $(-27)_{10}$ to an 8-bit binary number.

1B. Given the Boolean function f $(abcd) = a + \bar{a}\bar{b}c + \bar{b}\bar{d}$. Without minimizing, realize using
(i) Two input NAND gates
(ii) Two input NOR gates.

1C. Solve the following:
i. $(418.59)_{BCD} - (378.28)_{BCD}$, using 10's complement addition.
ii. $(1011.0101)_2 - (110.101)_2$, using 2's complement addition.

((2+2+2) + (3+3) +(5+3)=20 marks)

2A. Simplify the following expressions using Boolean algebra:

i. $F(abc) = \bar{a}\overline{b}\ \overline{c} + \bar{a}\overline{b}\,c + \bar{a}b\,\overline{c} + \bar{a}bc + a\overline{b}\ \overline{c} + a\overline{b}\ c + abc + ab\overline{c}$
ii. $F(ABC) = (A + B + \bar{C})(A + \bar{B} + \bar{C})(\bar{A} + B + \bar{C})(\bar{A} + \bar{B} + \bar{C})$
iii. $F(xyz) = \overline{x}\ \overline{y}\ \overline{z} + xz + \overline{y}\,z + xyz$

2B. Convert the following Boolean function $F(A, B, C) = (A + B)\left(\overline{B} + AC\right)(A + \overline{C})$ into SOP form, Canonical SOP form, POS form and canonical POS form.

2C. Explain features of 2 out of 5, 2421 and 24-2-1 BCD codes.

((2+2+2)+8+6=20 marks)

3A. Design BCD to Excess 3 converter using minimum logic gates.

3B. Design full subtractor using two input NOR gates.

3C. Realize the function $f(abcd) = \sum(0,2,5,7,8,9,13,14,15)$ using 8x1 multiplexer using least significant inputs as select lines.

(12+4+4=20 marks)

4A. Realize 16 to 1 multiplexer using 2 to 1 multiplexers. Also write the truth table.

4B. Using k-map, simplify the following Boolean functions in product of sum form and realize using logic gates.

(i) $f(wxyz) = \sum m(1,2,3,4,6,8,9,10,11)$.
(ii) $f(abcd) = \prod M(1,5,6,7,11,12,13,15)$

4C.Using 1 to 4 demultiplexer, implement 4 to 16 decoder as a max term generator.

(6+(4+4)+6=20 marks)

5A. Define the following terms with syntax, with respect to VHDL.

i. Process
ii. Variable
iii. Entity

5B. Explain OTPROM, EEROM, Flash, SRAM, DRAM, PSRAM, briefly.
5C. Write a VHDL code for four bit parallel adder using full adder as a component.

(6+6+8=20 marks)

6A. Derive characteristic equations for SR, JK, T and D flipflops.

6B. Using D-flipflops, design a mealy synchronous sequential circuit to detect an overlapping sequence 1010.

(10+10=20 marks)

7A. Design the four bit universal shift register using D flipflops and explain its operations.
7B. Using positive edge triggered JK flipflops, design mod 16 ripple counter which can be controlled to count up or down.

7C. Sketch a four bit Johnson's counter using D-flipflops. Draw the timing diagram.

(6+8+6=20 marks)

8A. Design Mod 8 synchronous up counter using JK flipflops. Also draw the timing diagram.

8B. Implement following Boolean functions using 3X 2 ROM:

$$f1(a,b,c) = \sum(1,2,4,6,7), \qquad f2(a,b,c) = \sum(1,3,4,5)$$

(12+8=20 marks)