Reg. No.										

INTERNATIONAL CENTRE FOR APPLIED SCIENCES

(Manipal University)

IV SEMESTER B.S. DEGREE EXAMINATION –MAY 2016

SUBJECT: MICROPROCESSOR SYSTEMS (EC 242)

(BRANCH: E& C / E&E)

27TH MAY, 2016

Time: 3 Hours **Max. Marks: 100**

- ✓ **Answer ANY FIVE full Questions.**
- ✓ **Missing data may be suitably assumed.**
- ✓ **Write comments or explain the logic for all the programming questions**

1A. Draw the block diagram of 8051 Microcontroller and explain briefly. List its features.

1B. With proper examples explain the following instructions of 8086 processor.
i) XCHG ii) DAA iii) AAM iv) XLAT v) ADC

(10+10)

2A. Explain the functions of the following 8086 pins. Mention if they are IN/OUT or Bi-directional signals.
a) $\overline{INTA}$ b) READY c) NMI d) $\overline{BHE}$

2B. With a neat diagram of the programming model of 8086, explain the function of all the registers explain the flag bits.

(8+12)

3A. Explain the following data definition directives with an examples and memory allocation sketches for each.
a) DB b) DW c) DD d) DT

3B. Write a program to multiple 2 two digit BCD numbers in 8086 and store the result in memory. The two BCD numbers are also in memory. Write comments or explain the logic for the program.

(10+10)

4A. Write down the steps for programming timer in mode 1. Write a program to display the two digit decimal down count with a delay of 0.5 seconds on port 1. Use timer 0 in mode 1 to generate delay crystal frequency= 11.0592MHz).

4B. Write I/O mode and BSR mode command word format of 8255. Write the control word to initialize 8255 as given below.
i) Port A input, port B output, port C lower input and port C upper output in mode 0.
ii) BSR mode to set and reset PC_5 line of port C.

(10+10)

5A. With a neat diagram, explain memory banking in 8086. Explain how even and odd addressed bytes and words are accessed in this memory configuration.

5B. Write a program to find GCD and LCM of two 8 bit numbers. Write comments or explain the logic for the program.

(10+10)

6A. With neat diagrams, explain memory write and I/O read bus cycles for the minimum mode operation of 8086.

6B. Explain briefly the steps taken by 8086 in response to an interrupt. Explain the interrupt vector table of 8086.

(10+10)

7A. It is required to interface two chips of 32K * 8 ROM and two chips of 16K * 8 RAM with 8086 according to the following map using a 74138 decoder. Design the required interfacing circuit.
ROM from F0000H and RAM from D0000H.

7B. With a neat diagram, explain internal architecture of 8051.

(10+10)

8A. Explain memory segmentation of 8086. List and briefly explain, advantages of segmentation.

8B. Explain memory architecture of 8051 with neat diagrams.

8C. Compare microprocessors and microcontrollers.

(10+5+5)