Reg. No.										

प्रज्ञानं ब्रह्म

Manipal

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INTERNATIONAL CENTRE FOR APPLIED SCIENCES

(Manipal University)

IV SEMESTER B.S. DEGREE EXAMINATION - MAY 2016

SUBJECT: VLSI DESIGN (EC 245)

(BRANCH: E & C)

23RD MAY, 2016

Time: 3 Hours **Max. Marks: 100**

- ✓ **Answer ANY FIVE full Questions.**
- ✓ **Layout must be drawn using the graph sheet provided.**
- ✓ **Missing data may be suitably assumed.**

1A. Explain the operation of pseudo NMOS inverter. Derive Zpu/ Zpd ratio for pseudo NMOS inverter driven from a similar inverter.

1B. Explain in detail about working of MOS capacitor.

1C.What do you understand by channel length modulation? Explain in detail.

(10+5+5)

2A.With the help of neat circuit diagram and curve, explain the working of CMOS inverter. Derive the expression for V_{inv}. Discuss the merits of CMOS inverter over NMOS inverter with depletion load.

2B. Calculate the effective capacitance for the given multi-layer structure in **Figure 2B** for 5µm process. Relative Capacitance value for metal1= 0.075, polysilicon=0.1 and Gate to channel = 1.0. (10+10)

3A. Explain the principle of photo lithography. Discuss the working of positive photo resist and negative photo resist with necessary diagrams.

3B. For a CMOS Inverter having$L_n = L_p = W_n = 2$ µm, $W_p = 5$ µm .Compute the following: (i) rise timet_r(ii) fall-timet_f (iii) total delay $T_d$through a pair of inverters. Given the typical sheet resistance and standard capacitance values for 2 µm process: [i] NMOS channel resistance = 20 kΩ/square [ii] PMOS channel resistance = 45 kΩ /square[iii] Gate-to-channel capacitance = 8pF x 10^{-4}/um^2.

3C. With neat figures explain the different steps involved in the fabrication of NMOS transistor. What is the advantage of self-aligned process? (5+5+10)

4A. Draw the circuit, stick diagram and layout for two input CMOS EXNOR gate.

4B. Implement 2 input NAND and NOR functions using following approach: [a] pass transistors, [b] Transmission gates, [c] NMOS logic with depletion load, [d] CMOS logic

(10+10)

5A. Give the circuit implementation of following multiple output function using NMOS based PLA. Give the stick notation. $Z_1 = AB + \bar{A}\bar{B}C$; $Z_2 = AB$; $Z_3 = A + \bar{B}C$.

5B. Give hardware implementation for storing following 4-bit words using NMOS ROM structure. word1: 0101 ; word2: 0010 ; word3: 1001 ; word4: 0110

5C. Calculate I_D and V_{SD}, and indicate region of operation of transistor M1 for the circuit in **Figure 5C**. *Vtp* = –0.4 V, *Kp* = 120 $\mu A/V^2$, and *W*/*L* = 2. (5+5+10)

6A. Discuss the structured design implementation of (n+1)-bit parity indicator block that is provided with $n+1$ bit input word $A_n A_{n-1} A_{n-2} \ldots . A_1 A_0$. The circuit has one bit parity output P. P will be HIGH (LOW) for even (odd) number of 1s at input. Give the stick notation for CMOS implementation of standard cell.

6B. i)With the help of a neat circuit diagram, explain the operation of BiCMOS inverter. Also highlight the role of each transistor in the circuit.
ii)What are the merits and demerits of the BiCMOS logic. (10+10)

7A. Compare and contrast CMOS, bipolar and GaAs technologies.

7B. Discuss cascaded inverters as drivers for driving large capacitive loads and derive the necessary expressions. (10+10)

8A. Explain the fabrication process of DMESFET using planar technology with necessary diagrams.

8B. Explain different scaling models. Discuss the effect of different scaling on following parameters: [i] Gate oxide capacitance C_g[ii] Channel resistance R_{on}
[iii]Gate delay T_d (10+10)

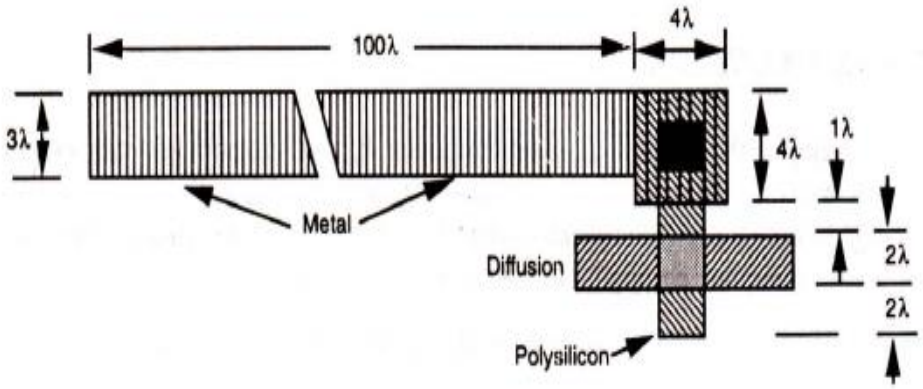

Figure 2B

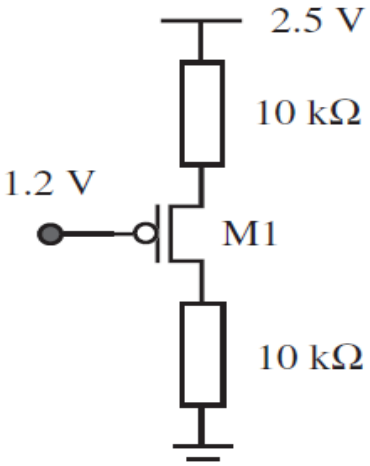

Figure 5C