Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

(A Constituent Institute of Manipal University)
Manipal – 576 104

IV SEMESTER B.Tech.(BME) DEGREE MAKEUP EXAMINATIONS JUNE/JULY 2016
SUBJECT: DIGITAL SYSTEM DESIGN (BME 2203)
(REVISED CREDIT SYSTEM)
Tuesday, 5th July 2016: 2 pm to 5 pm

TIME: 3 HOURS **MAX. MARKS: 100**

Instructions to Candidates:

1. **Answer all FIVE full questions.**
2. **Draw labeled diagram wherever necessary**

1. (a) What is a "*Semicustom IC*" and explain. How it is different than a standard IC. **07**

(b) Draw the "Y-chart" and explain it considering a digital system, either referring to BOTTOM UP or TOP DOWN design. **08**

(c) Give the difference between TTL and CMOS gates. Draw the circuit of a CMOS inverter gate and explain. **05**

2. (a) Describe the major process steps which are considered during the fabrication of NMOS transistor. **08**

(b) Realize the following (as per the given specification):
(i) Implement the function $F1 = AB + AC + BC$; using OAI logic.
(ii) Implement the function $F2 = (A' + B)(C + D')$; use AOI logic **06**

(c) Draw the circuit of a CMOS NOR circuit and explain its operation. **06**

3. (a) What is Application Specific Integrated Circuits (ASICs)? What are its benefits and the limitations? **04**

(b) Explain how Programmable Logic Array (PLA) device is different than Programmable Array Logic (PAL) device? Design a full adder circuit using PLA device. **08**

(c) Explain architecture of *Field-Programmable Gate Arrays (FPGAs)* along with the following details: **08**

(i) Configurable logic block

(ii) Switch Matrix

4. **(a)** Explain how FPGA is different than other simple programmable logic devices (PLDs). **04**

(b) Write a Verilog HDL code for synthesizing the following: **10**

i. 2 to 4 Decoder

ii. Full Adder

(c) Describe "behavioral style" of digital system design using Verilog HDL with an example. **06**

5. **(a)** What is VLSI technology? Explain classification ICs based on integration. **06**

(b) Explain the following: **06**

(i) **always** @(……) statement

(ii) **and** A (z1,x,y); statement

(iii)`**timescale** 10ns/10ns

(c) Define Shannon's theorem for realisation of digital hardware. Expand the function, **08**

$F = \bar{W_1}\,\bar{W_3} + W_1W_2 + W_1W_3$ using Shannon's theorem and implement it using a multiplexer: