Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

(A Constituent Institute of Manipal University)
Manipal – 576 104

IV SEMESTER B.Tech.(BME) DEGREE END SEMESTER EXAMINATIONS MAY 2016
SUBJECT: DIGITAL SYSTEM DESIGN (BME 2203)
(REVISED CREDIT SYSTEM)
May 12th , Thursday, 2016, 2 to 5 PM

TIME: 3 HOURS **MAX. MARKS: 100**

Instructions to Candidates:

1. **Answer all FIVE full questions.**
2. **Draw labeled diagram wherever necessary**

1. (a) What is a fully customized Application Specific Integrated Circuit (ASIC)? Explain the ASIC design flow. 07

   (b) What is "TOP-DOWN" design methodology? Explain the approach with an example of a 4-bit ripple adder. 08

   (c) What is the major benefit of CMOS technology, when compared to nMOS or pMOS ? Design a two input NAND gate using Complementary MOS transistors. 05

2. (a) What is *Algorithmic State Machine* (ASM)? Explain the design of a bus arbiter system controller using an ASM chart and ASM table. 08

   (b) Design a 2:1 multiplexer using two transmission-gates and an inverter gate. Explain its operation. 06

   (c) Design a 4x4 multiplier using full adders and half adders as a major elements. Estimate the time required to generate a product in terms of gate propagation delay. 06

3. (a) Explain the advantage of Programmable Logic Devices (PLDs), and how these devices are classified? 04

   (b) Describe the general architecture of the Programming Array Logic (PAL) device. Consider a function $X = A'C + A'D' + BC + BD'$, which has four input variables. Realize the function, configuring the PAL device. 08

(c) What is a "coarse grained" *Field-Programmable Gate Arrays (FPGAs)?* With a neat diagram, explain the general architecture of FPGA. 08

4. (a) Define *Complex Programmable Logic Device* (CPLD) and explain how it is different from a MPGA. 04

(b) Write a Verilog HDL code for synthesizing the following:

i. D Flip-flop 10

ii. 4:1 MUX

(c) Give the syntax of "always" statement with the "blocking" style. Explain how it is different from the "non-blocking" style of Verilog HDL design. 06

5. (a) What are *Gate Array Based ASIC*s? Explain *channeled Gate Array ASIC* and *channel less Gate Array ASIC*. 06

(b) Write a Verilog HDL code for implementing a "4-bit adder", using four full adders. Note: Design the full adder module using structural style. 06

(c) Expand the given function (*f*) using Shannon's expansion theorem: $f = x_1'x_2' + x_1x_2$. Realize it using 2 input LUT (Look Up Table). 08