Reg. No.									

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

IV SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, MAY 2016

SUBJECT: ANALOG SYSTEM DESIGN [ELE 2204]

REVISED CREDIT SYSTEM

Time: 3 Hours | 14 MAY 2016 | MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitable assumed.

1A. For the circuit shown in Fig. Q1A, determine the voltage v_1, v_2 and v_o. ***03***

1B. Using one op-amp, powered from ±12 V regulated power supplies, design a circuit to yield $v_o = 5(V_2 - V_1) - 8$, where V_1 and V_2 are input voltages. Assume feedback resistance as 10 kΩ. ***03***

1C. Using op-amps, develop a circuit schematic to monitor the voltage level of battery under the following conditions:

i. $V_i \leq 4$ V and $V_i \geq 10$V, **Red** LED needs to be ON otherwise remain OFF

ii. $6 \leq V_i \leq 10$V, **Green** LED ON otherwise OFF

Briefly explain the working of the circuit. ***04***

2A. For a practical integrator, if the component values are R_1 = 10 kΩ, R_f = 100 kΩ, C_f = 0.1 μF, determine: a) the gain of the circuit at f= 0 Hz. b) lower frequency limit of integration, c) unity gain frequency. ***03***

2B. Briefly discuss the advantages of negative feedback over positive feedback. ***02***

2C. Using pole-zero concept, design an op-amp based Butterworth filter which can pass frequencies upto 10 kHz. It is expected to have a transition band gain roll-off of 60 db/decade. Assume C = 0.1 μF and feedback resistor R_f = 1 kΩ. Evaluate the overall gain in the pass band. Also, derive the Butterworth polynomial equation. ***05***

3A. Design an op-amp based circuit to introduce a delay of 75 μs between the input and the output when the frequency of input signal is 2 kHz. Use capacitor of 0.1 μF, if required. ***03***

3B. Draw the circuit for an op-amp based zero crossing detectors. Hence plot the output with respect to time when the input is a sinusoidal signal. ***02***

3C. What are the conditions to be satisfied to obtain sustained oscillations? With a neat op-amp based circuit, derive expression for the frequency of oscillation of a RC phase shift oscillator. Also comment on the gain of the circuit. ***05***

4A. Design an op-amp based circuit to get the voltage transfer characteristics as shown in Fig. Q4A. Assume feedback resistor to be 10 kΩ. Hence plot the output with respect to time when the input is given by $v_i(t) = 15 \sin \omega t$. Use minimum number of components. ***04***

4B. Design a 555 timer based monostable multivibrator circuit to produce a pulse of 3 ms. Also, design a negative edge trigger circuit to trigger the monostable circuit by a 500 Hz square wave and hence draw the waveforms at pin 6 and pin 3. Assume all the capacitors to be 0.1 μF. ***03***

4C. With the help of a block schematic, explain the working of a PLL. Also discuss the capture range and lock range of PLL. ***03***

5A. With a neat circuit schematic, explain the working of precision full-wave rectifier. ***02***

5B. Derive the expression for the input and output resistance of a transresistance amplifier with feedback. ***04***

5C. Draw the equivalent open loop small signal circuit for the amplifier circuits shown in Fig.Q5C (i) and Fig.Q5C (ii). ***04***

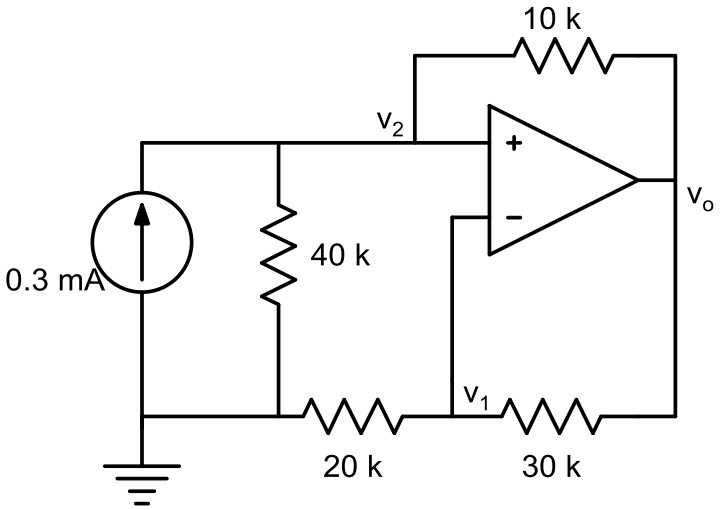

Fig.Q1A

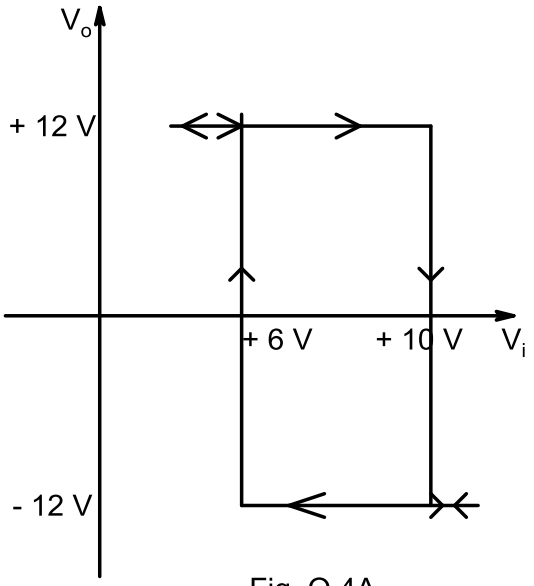

Fig. Q 4A

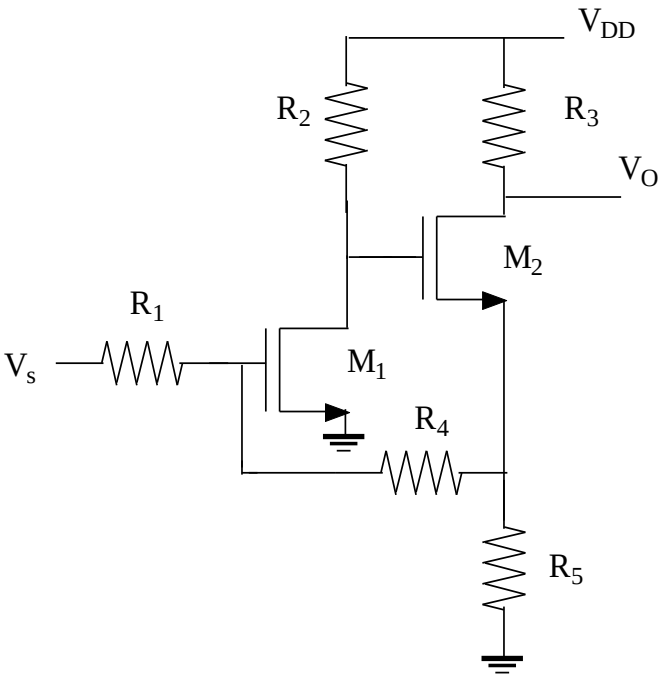

Fig.Q5C (i)

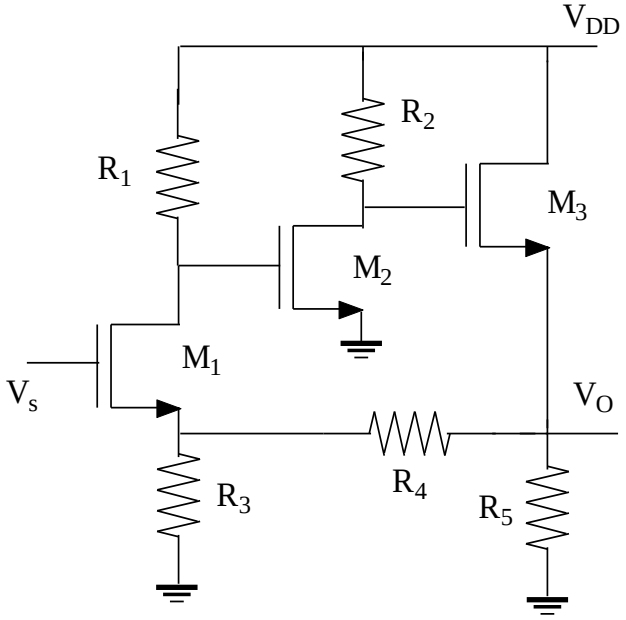

Fig.Q5C (ii)