Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

IV SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

MAKEUP EXAMINATIONS, MAY 2016

SUBJECT: DIGITAL SYSTEM DESIGN & COMPUTER ARCHITECTURE [ELE 2203]

REVISED CREDIT SYSTEM

Time: 3 Hours | 05 JULY 2016 | MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL th**e questions.
- Missing data may be suitable assumed.

1A. Briefly explain the Implementation options of digital system. ***(03)***

1B. Write Verilog code to implement a 4 to 2 priority encoder, using gate level primitives. Ensure that the resulting circuit is as simple as possible. ***(03)***

1C. Write a Verilog function for a 2 to 4 decoder. Using this as a component, implement a 4 to 16 decoder. ***(04)***

2A. Write a Verilog code for a 4 bit full adder using Generate statement. ***(04)***

2B. Write a Verilog code for a modulo 12 up counter with synchronous reset. ***(03)***

2C. Write a Verilog HDL code to generate 1 Hz square wave from 10 KHz clock signal. ***(03)***

3A. Write a Verilog Code for a 4 bit ALU which performs the following functions. Use Case Construct for the design

Select Input	Operation
00	A+B
01	A-B
10	A AND B
11	A OR B

(04)

3B. Draw the state diagram for the sequence detector 111 and 000 using Moore machine and write the Verilog HDL code for it. ***(04)***

3C. Implement 8 to 1 mux using PLA by considering appropriate size for the inputs and gate planes. ***(02)***

4A. Perform $45_{(10)}$*-$60_{(10)}$ using Booth's algorithm. ***(04)***

4B. With a neat diagram, explain briefly the priority handling concept of Polled Interrupts. ***(03)***

4C. For a 6 segment floating point pipeline the propagation delays of the segments are Given below.

T1=100ns,T2=120ns,T3=60ns,T4=50ns,T5=180ns,T6=40ns,Tlatch=20ns;

i. Determine the pipeline clock rate.

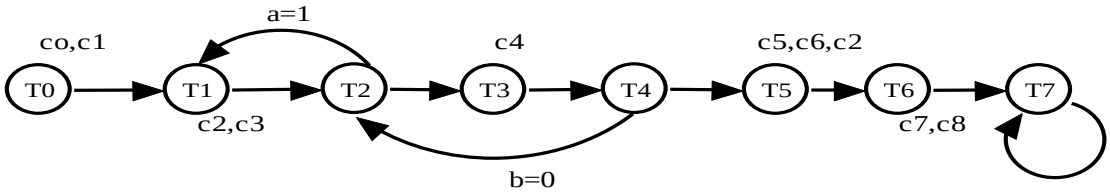
ii. Find the time taken to add 1000 pairs of floating point numbers using this pipeline.

iii. Determine the efficiency of the above pipeline. ***(03)***

5A. Draw the block diagram of the micro programmed control unit to implement the following state diagram.

I. Write the micro program for the same.

II. What is the size of the control memory?



(04)

5B. Explain the different mapping techniques in Cache memory with diagrams. ***(06)***