Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

IV SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, MAY, 2016

SUBJECT: DIGITAL SYSTEM DESIGN & COMPUTER ARCHITECTURE [ELE 2203]

REVISED CREDIT SYSTEM

Time: 3 Hours 12 MAY 2016 MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** questions.
- Missing data may be suitable assumed.

1A. i) Write a technical note on

a) Czochralski crystal growth b) photolithography.

ii) List 4 FPGA programming Technologies. ***(03)***

1B. Write Verilog code to implement the function f (x1, x2, x3, x4) = $\sum m(1,2,4,5,6,7,8,10)$ using the gate level primitives. Ensure that the resulting circuit is as simple as possible. ***(02)***

1C. Implement a 4 bit Excess 3 to BCD code converter using 3 to 8 decoders and residual gates. Write a function for 3 to 8 decoder. Using this function, write Verilog code for the code converter. ***(05)***

2A. Write the Verilog code for a configurable n:1 multiplexer ***(03)***

2B. Write a behavioral Verilog code for a presettable counter which counts from 3 to 13, with asynchronous active low clear and negative edge triggered clock. ***(04)***

2C. Write a behavioral Verilog HDL code for a 8 bit Universal Shift register, with the following specifications. i) Synchronous , active high Clear ii) negative edge triggered clock

S1	S0	Operation
0	0	Hold the previous data
0	1	Right shift by 1 bit, with **rin** as right serial input
1	0	Left Shift by 1 bit, with **lin** as left serial input
1	1	Load the 8 bit data

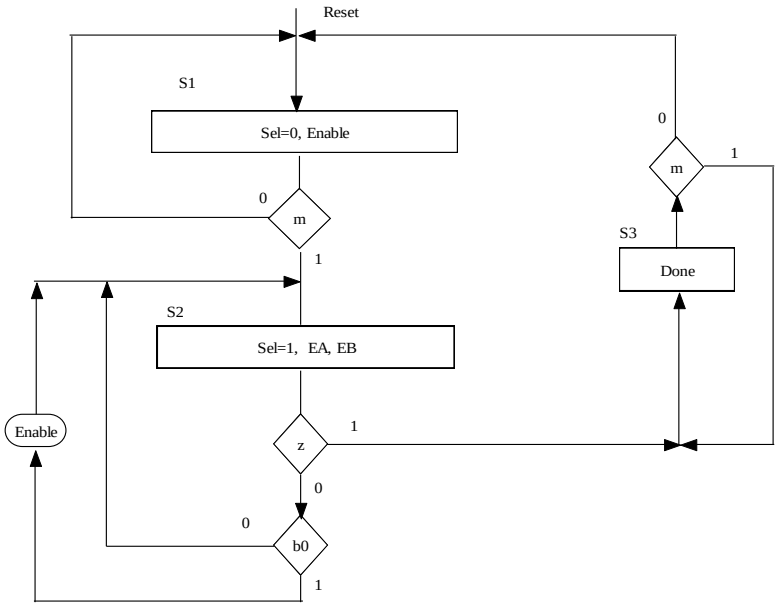
(03)

3A. Draw the circuit for the Verilog code given below:

```
always @(posedge Clock)
begin
Q1 = D;
Q2 = Q1;
end
endmodule
```

Rewrite the complete code with port declarations, using nonblocking assignment. Draw the synthesized circuit for the same. ***(04)***

3B. Write a behavioral Verilog code for the ASM chart shown.



(04)

3C. Implement f (a,b,c)= ΠM(1,2,4,7) and Z(a,b,c) = $\sum m(1,2,4,7)$ using PLA. ***(02)***

4A. Given an instruction set and the corresponding relative frequency, encode using Huffman's method and calculate the redundancy.

Instruction	I0	I1	I2	I3	I4	I5	I6	I7
Relative frequency count	0.01	0.05	0.15	0.01	0.09	0.07	0.29	0.33

(03)

4B. Perform 60_H /15_H by non restoring division algorithm. ***(04)***

4C. Assume main memory has 4 page frames and initially all page frames are empty. Consider the following stream of references: 1,2,6,2,1,4,5,3,1,4,5,3 Calculate the hit ratio when the following types of replacement policies are used.

i)FIFO ii) LRU ***(03)***

5A. Given the register transfer description, develop the control signals and design the processing section for the following algorithm, using Hardwired approach

Declare registers: A[4] ,M[4], Q[5], L[3];
Declare buses: In bus[4],Out bus[4];

Start : A ← 0, M ← Inbus, L ← 0100;
Q[4:1] ← In bus, Q[0] ← 0;

Loop: if Q[1:0] = 01 then goto ADD;
if Q[1:0] = 10 then goto SUB;
goto RShift;

ADD: A ← A+M ;
Goto RShift;

SUB: A ← A-M ;

RShift: Arithmetic Right Shift content of AQ register, L←L-1;
If L<>0 then go to loop
Outbus=A;
Outbus=Q[4:1];

Halt: Go to Halt. ***(07)***

5B. Consider 850 X 90 bit microprogram stored in a single memory and 300 out of 850 instructions are unique. Find the savings in bits if nanomemory is used instead of a single memory store. ***(03)***