| Reg. No. | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

**FOURTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION**
**MAY/JUNE 2016**
**SUBJECT: Digital System Design & HDL (ECE - 206)**

**TIME: 3 HOURS** **MAX. MARKS: 50**

**Instructions to candidates**
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. Write a structural VHDL code for a four bit carry ripple adder.

1B. Explain the signature analysis technique with an example.

1C. Explain the SRAM programming technology with diagram.

(5+3+2)

2A. Write a structural VHDL code for a 3 bit ripple up counter using T flip-flops.

2B. Implement full adder using ACT-3 C Module. Show the relevant design steps.

2C. If A = 111, B = 011 and C = 010, what are the values of the following statement?
(a) (A & B) or (B & C)
(b) A & B

(5+3+2)

3A. Find test vector for the circuit shown in FIG. 3A using i) D algorithm ii) PODEM

3B. Implement synchronous 3 bit down counter using PAL with 2 wide OR array plane and D flipflop.

3C. Find the reduced fault set for a two input OR gate.

(5+3+2)

4A. Find the test vector for the circuit shown in FIG. 4A sing ITG method.

4B. Write a behavioural VHDL code for an 8-to-1 MUX with active-low output and active-high enable input.

4C. Draw diagram for ACTEL ACT 2 C Module.

(5+3+2)

5A. Write a behavioural VHDL code for 1010 overlapping sequence detector.

5B. Write a structural VHDL code for a full adder using basic gates.

5C. Explain any two Ad-hoc DFT techniques with examples.

(5+3+2)

6A. Implement BCD to Excess -3 code converter using Xilinx XC3000 FPGA. How many CLBs and LUTs

required? Show the contents in the SRAM cell?

6B. Find the test vector for the fault shown in FIG. 6B using Boolean difference method.

6C. Write a behavioural VHDL code for a 2-to-4 decoder with active high *enable* input.

(5+3+2)

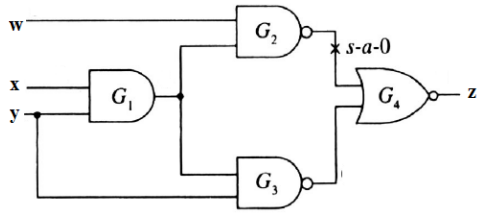


**FIG. 3A**

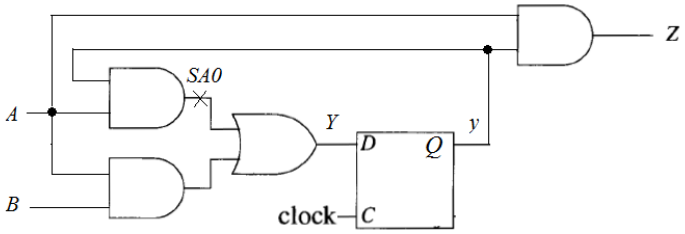


**FIG. 4A**

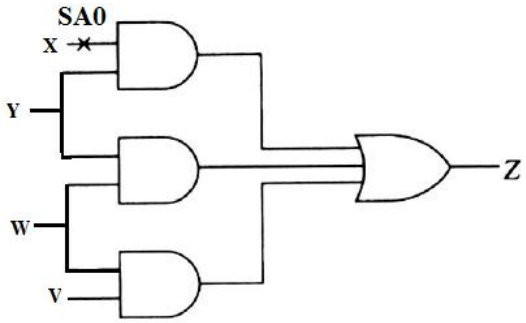


**FIG. 6B**