Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FOURTH SEMESTER B. Tech. (E & C) DEGREE END SEMESTER EXAMINATION
MAY/ JUNE 2016
SUBJECT: DIGITAL SYSTEM DESIGN USING VERILOG (ECE - 2204)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Implement following functions using Xilinx XC 3000. How many CLBs and LUTs are required?

$\mathbf{Y_1 = \bar{x} + y_1}$; $\mathbf{Y_2 = x\,\overline{y_2} + \bar{x}\,\overline{y_1}}$; $\mathbf{z = x\,.\,y_1}$ where $\mathbf{Y_1, Y_2}$ are the next state variables and $\mathbf{y_1}$, $\mathbf{y_2}$ are the present state variables. Here, **x** and **z** are input and output respectively.

1B. Draw and explain Gajski's Y chart.

1C. What is the disadvantage of shared expanders in Altera MAX architecture?

(5+3+2)

2A. Give implementation of [i] 3 bit Johnson counter using ACT2 LM [ii] SR latch using ACT1 series.

2B. Explain ASIC design flow.

2C. Find the fault collapse ratio of a three input NAND gate using both fault equivalence and fault dominance relation.

(5+3+2)

3A. [i] Find the test vector for SA1 fault in the circuit FIG. 3A using ITG. [ii] Find the test vector for SA0 fault at input node **y** in the circuit FIG. 3B using Boolean difference method.

3B. Illustrate the use of muxes to increase the access to internal nodes with an example.

3C. What are the steps involved in path sensitization based ATPG? Explain with an example.

(5+3+2)

4A. Write a Verilog code for positive edge triggered D flip-flop using primitive.

4B. Write a structural Verilog code for a 4-bit ripple counter using negative edge triggered T flip-flop as building block.

4C. Differentiate blocking and non-blocking procedural assignment statements with example.

(5+3+2)

5A. Write a sequential Verilog code for Mod 100 counter.

5B. Write the switch level Verilog HDL code for CMOS inverter.

5C. Write the structural Verilog HDL code for Half-adder using only NAND gates [minimal implementation preferred]

(5+3+2)

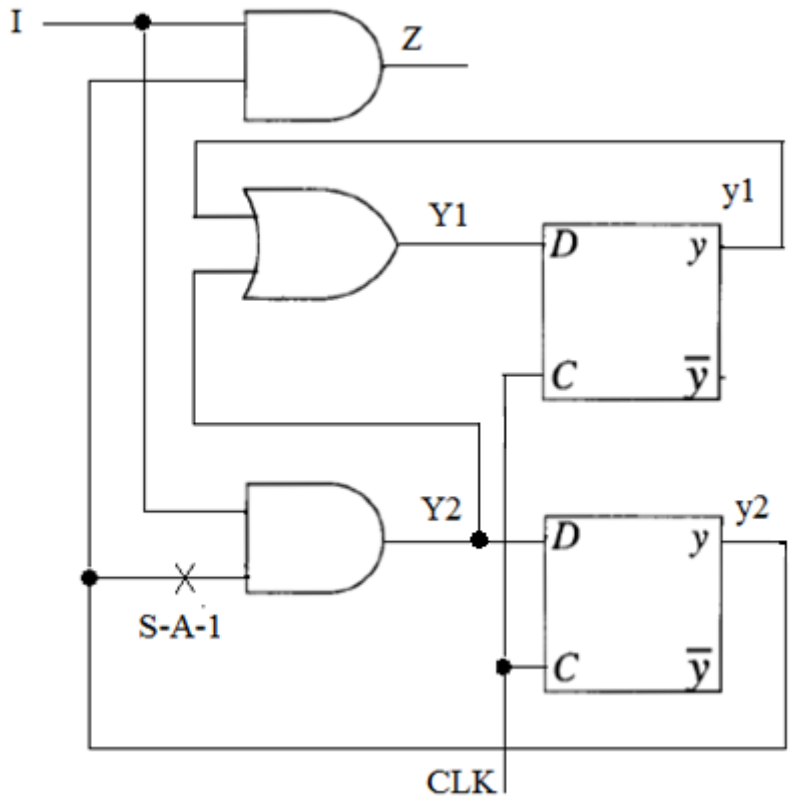

FIG. 3A

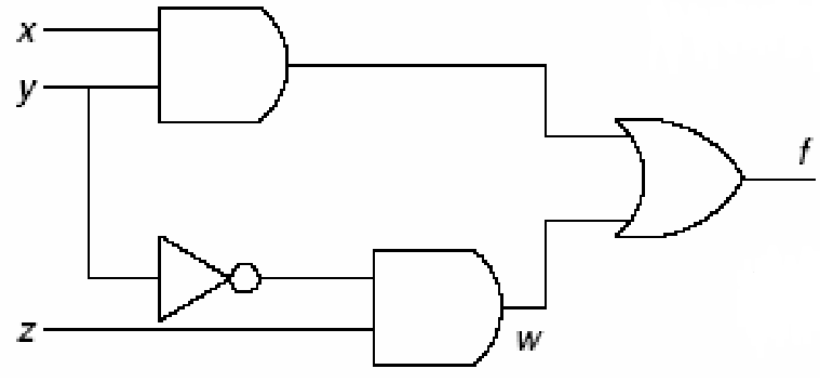

FIG. 3B