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MANIPAL INSTITUTE OF TECHNOLOGY  
Manipal University



**FOURTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION  
MAY/ JUNE 2016**

**SUBJECT: DIGITAL SYSTEM DESIGN USING VERILOG (ECE - 2204)**

**TIME: 3 HOURS**

**MAX. MARKS: 50**

**Instructions to candidates**

- Answer **ALL** questions.
- Missing data may be suitably assumed.

- 1A. Implement 3 bit binary- to-gray code converter using ACT1 series
- 1B. Explain the following terms: [i] channeled and channelless gate array [ii] Logic Synthesis [iii] antifuse switch
- 1C. Compare ASIC and FPGA.
- (5+3+2)
- 2A. Find the test vector for SA0 fault shown in **FIG. 2A** using ITG
- 2B. Implement following function using Xilinx XC 3000. How many CLBs and LUTs are required?  
 $F(a,b,c,d,e) = a.b.c + a.\bar{b}.c + \bar{e} + d.e$
- 2C. Find the test vector for SA1 fault at node  $\alpha$  shown in **FIG. 2C** using D-Algorithm
- (5+3+2)
- 3A. Find combinational controllability and observability measures of all the nodes for the circuit in **FIG. 3A**.
- 3B. Obtain the minimal test vector set for the fault set {a0, b0, c0, d1, e0, f1} in the circuit of **FIG. 3B** using fault table method.
- 3C. How will you enhance the observability of node  $\alpha$  in the circuit of **FIG.3C**.
- (5+3+2)
- 4A. Write a sequential Verilog code for 4-bit Carry Look Ahead (CLA) adder.
- 4B. Find the test vector to detect the fault SA1 at node  $\alpha$  for the circuit in **FIG. 4B** by path sensitization method.
- 4C. Give a data-flow Verilog model for 3-to-8 decoder with enable input and active high output.
- (5+3+2)
- 5A. Write a structural Verilog code for 4 bit carry ripple adder (CRA) using 1-bit full adder module.
- 5B. Write the switch level Verilog HDL code for two-input CMOS NAND gate.
- 5C. Implement the following expression using Altera MAX FPGA having 3 wide AND OR array plane.  $F = AB\bar{C} + \bar{A}\bar{B} + \bar{B}C + \bar{A}\bar{D} + AB\bar{D}$
- (5+3+2)

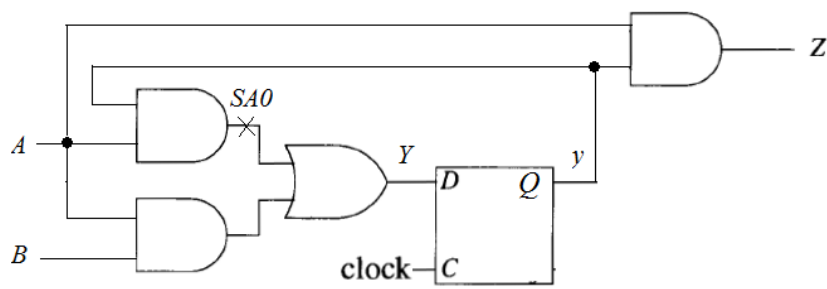


FIG. 2A

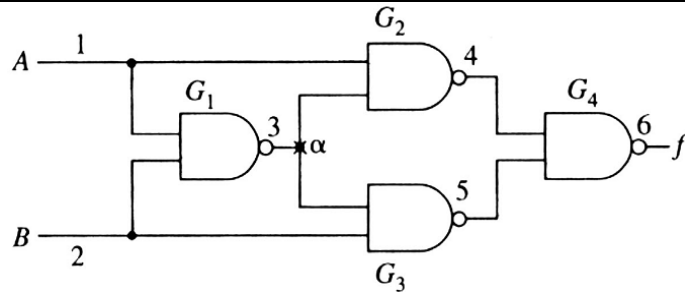


FIG. 2C

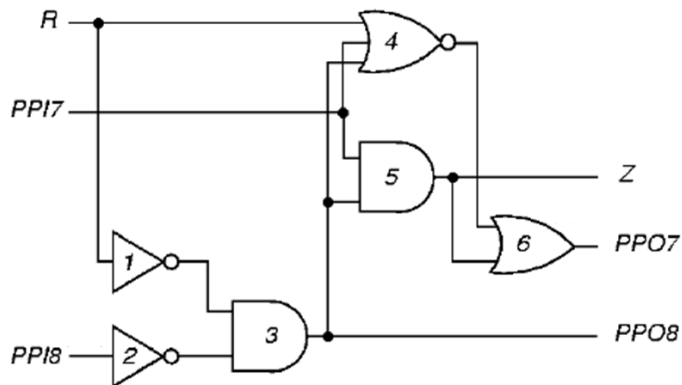


FIG. 3A

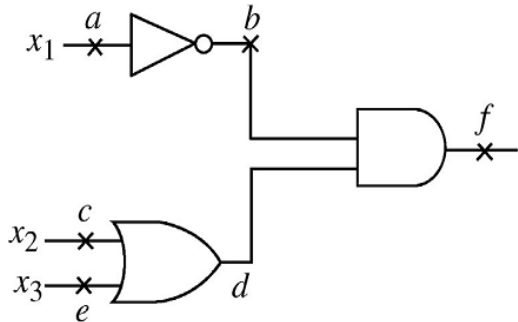


FIG. 3B

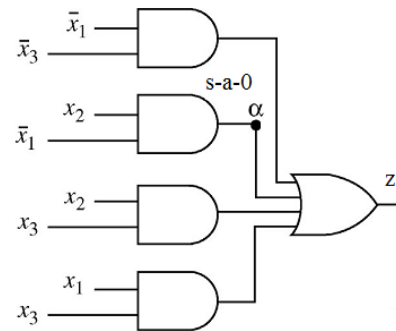


FIG. 3C

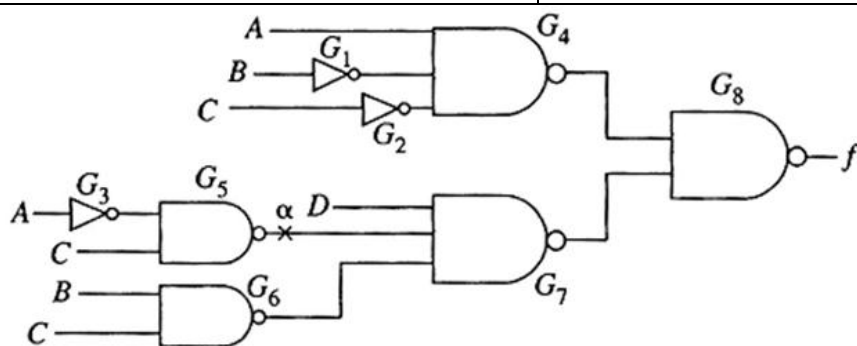


FIG. 4B