Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FOURTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION
MAY/JUNE 2016
SUBJECT: I C SYSTEMS (ECE - 2202)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Draw the circuit of an emitter coupled differential pair using BJTs and derive the expression for the CMRR.

1B. Define the following terms related to Op-amp and indicate their significance: i) Slew rate ii) Unity gain bandwidth and iii) input bias current

1C. Draw the circuit of output stage of an op-amp and explain the operation.

(5+3+2)

2A. Design a circuit to perform following function using minimum number of Op-amps.

i) $V_0 = (V_1 * V_2)$

ii) $V_0 = (V_1 + V_2 + V_3)/3$

2B. Draw the circuit of a full wave precision rectifier and illustrate the operation using suitable analysis.

2C. Draw the circuit of peak detector and explain the operation.

(5+3+2)

3A. Design a second order Butterworth active band pass filter to pass frequencies in the band 5kHz and 10kHz.

3B. Design a suitable circuit to remove 100 Hz frequency component from the input signal. The quality factor of the circuit should be 20.

3C. List the key desirable characteristics for an instrumentation amplifier.

(5+3+2)

4A. Design a practical integrator with peak gain of 10 and -3dB frequency is 200Hz. Assume a capacitance of 0.1µF. Draw the relevant frequency response showing salient values. Assuming a square wave of peak to peak 1 Volt and frequency of 1kHz is applied to this integrator; sketch the output waveform showing relevant magnitudes and timings.

4B. Design a suitable circuit using 555 timer to generate a pulse train of 1kHz, peak voltage of 10 V and

duty cycle of 40%.

4C. Design a 555 Timer based circuit to generate FSK signal. Assume data rate to be 200Hz, and the output FSK should have frequencies 1070 Hz. and 1270 Hz.

(4+3+3)

5A. Draw the circuit of an 8-bit flash ADC and explain the working.

5B. With the help of suitable circuit explain the operation of R-2R ladder type DAC.

5C. With the help of a block diagram explain the operation of PLL.

5D. Design op-amp based circuit to generate a triangular waveform of 1kHz.

(2.5 X 4) = 10)