Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FOURTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION
MAY/JUNE 2016
SUBJECT: I C SYSTEMS (ECE - 2202)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Design the differential amplifier circuit shown in **Fig. 1A**, if the required A_d is 50 and CMRR is 40dB. Assume V_{cc} = 10 volts, $V_{A1} = V_{A2} = \infty$, V_{BE4} = 0.75V, β =100 for all transistors and collector current of transistor Q3 is 2mA.

1B. Explain with the help of suitable circuits and analysis how the CMRR of a differential amplifier can be improved.

1C. Explain the need for level shifters in op-amps and illustrate the action of level shifting using any two level shifter circuits as examples.

(4+3+3)

2A. Using block schematic show how analog multipliers and dividers can be implemented. Also show the circuit implementation of basic building blocks.

2B. Design a circuit to implement the equation $V_0 = (2V_1 - 3V_2)/2$, using minimum number of op-amps. (V_1 and V_2 are inputs and V_0 is output)

2C. Design a circuit using single op-amp to implement the equation $V_0 = 1/RC \int V_i \, dt$.

(4+3+3)

3A. Analyse the circuit shown in **Fig. 3A**, and get the expression for the output. Comment on the function performed by the circuit.

3B. Design an active Butterworth high pass filter with a cut off frequency of 5kHz and -60dB/decade roll off in the transition band.

3C. Draw a circuit for implementing sample and hold operation and explain the circuit operation.

(5+3+2)

4A. Design an active narrow band pass filter to meet the following specifications: f_0 = 1kHz, Q=12, A_F = 20. If the centre frequency needs to be shifted to 1.5kHz, keeping the gain and bandwidth same, what needs to be done?

4B. Design a Schmitt trigger circuit using op-amp with the following specification

UTP=3V

LTP=1V

Vout=+10V or -10V. (Assume +/- Vsat = 14Volts)

4C. With the help of a neat block diagram explain the operation of frequency multiplier using PLL.

(4+3+3)

5A. With help of suitable circuit and expressions, explain the operation of Dual slope ADC.

5B. In an 8 bit dual slope ADC, if maximum input is 12V and maximum integrator output is -8V, determine the value of resistance required. Assume a capacitor of 0.1uF and clock frequency of 4MHz is used. Also find out the digital code for an analog input of 5.125V using above parameters.

5C. If in an 8-bit DAC, the reference voltage used is 12 volts, calculate i) the resolution ii) the full scale output voltage and iii) the output voltage corresponding to the binary input of 10000000

5D. Design a circuit to generate a ramp signal of 5kHz using 555 Timer.

(2.5 X 4 = 10)

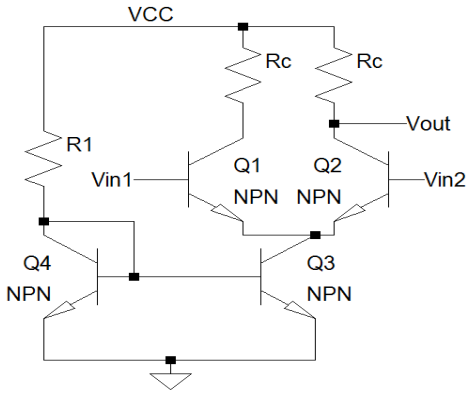

Fig. 1A

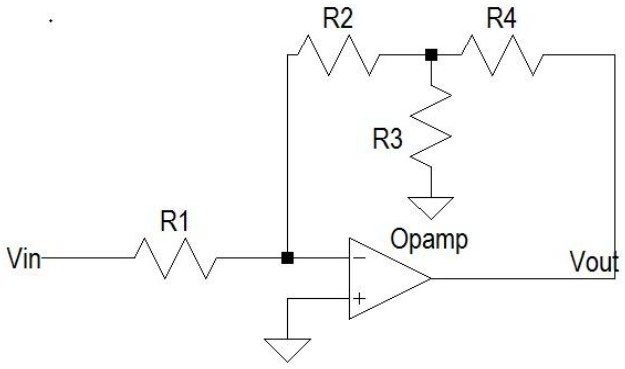

Fig. 3A