Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FOURTH SEMESTER B. Tech. (E & C) DEGREE END SEMESTER EXAMINATION
MAY/JUNE 2016
SUBJECT: IC SYSTEMS (ECE - 202)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. For the circuit in **Fig. 1A**, $R_{c1} = R_{c2} = 4.7\ k\Omega$, $R_E = R_{s1} = R_{s2} = 1\ k\Omega$, determine the value of A_C, A_D and CMRR. Assume identical transistors with $h_{fe} = \beta = 100$ and $h_{i\ e} = 1\ k\Omega$. Neglect other parameters of BJT.

1B. With the help of a circuit diagram and analysis, explain how a constant current bias circuit improves the CMRR of an emitter coupled differential amplifier.

1C. For the circuit shown in **Fig. 1C**, determine the value of I_0 for β=100. Assume V_{BE}=0.7 V.

(5+3+2)

2A. Using single Op-amp, design a suitable circuit to solve the following equation.

$V_0 = 3V_1+V_2-2V_3-7V_4-V_5$. (Do not invert the inputs)

2B. For the circuit shown in **Fig. 2B** find V_0/V_I. If the individual Op-amps saturate at ±13V, what will be the peak-to-peak value of output voltage.

2C. For a non-inverting integrator shown in **Fig. 2C** show that $V_{out} = \frac{1}{RC}\int V_{in}\ dt$ using an ideal Op-amp, R_1=R_2 and C_1=C_2.

(5+3+2)

3A. With the help of an OP-AMP based circuit diagram and analysis explain voltage to current converter with (i) Floating load and (ii) Grounded load.

3B. Design a second order narrow RC band pass filter for the following specifications:

Mid band voltage gain = 34dB
Quality factor = 10
Band width = 16Hz

3C. Design a circuit using single OPAMP to obtain output $V_0 = V_1 - 2V_2$ where V_1 and V_2 are the inputs.

(5+3+2)

4A. Design an OPAMP based square wave generator for the following specifications:
Frequency of oscillation = 1 kHz, Duty cycle = 25%
β = 0.5, Select C = 0.01μF .
Also sketch the voltage waveform across the capacitor and output.

4B. Design an inverting Schmitt trigger for the following specifications:
V_{UT} = 5V, V_{LT} = -2V
$+V_{CC} = -V_{EE}$ = 12 V.

4C. Draw the circuit diagram of peak detector and explain its working

(5+3+2)

5A. Design a 5-bit binary weighted resistor type DAC whose full-scale output voltage is -12V. Logic level 1=+5V&Logic level 0=0V. Determine the output when the input is (i) 11010 (ii) 10111. What is the resolution of the DAC designed? Select R=10 kΩ.

5B. With the help of a block diagram, explain the operation of an 8-bit successive approximation type ADC, for converting an analog input signal of 4.5V to a corresponding digital output. Assume the full scale output is 12V.

5C. Design a circuit to produce pulse width of 30 ms using IC 555.

(5+3+2)

6A. Draw the internal circuit diagram of IC 566 and explain its working. With the help of suitable wave forms, derive the expression for output signal frequency

6B. Define the following terms (i) free running frequency (ii) Lock Range (iii) Capture Range.

6C. Explain how PLL can be used as frequency divider

(5+3+2)

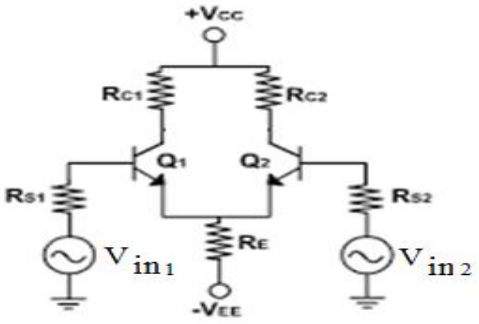

Fig.1A

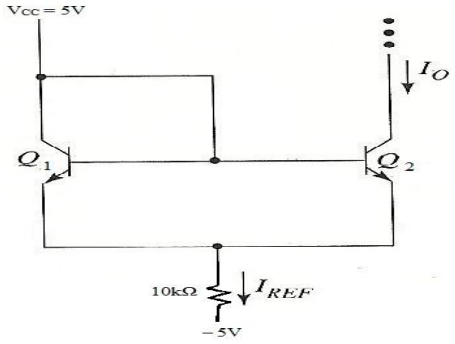

Fig. 1C

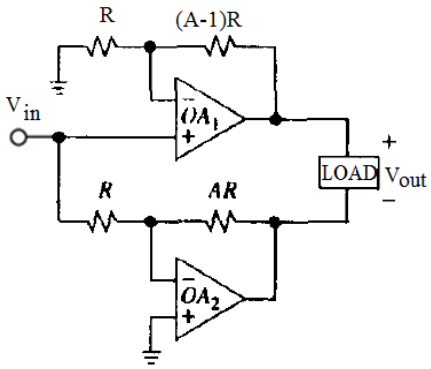

Fig. 2B

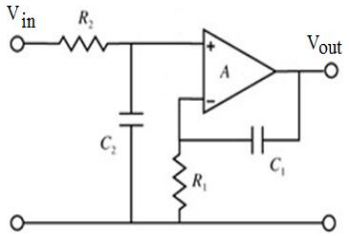

Fig 2C