Reg. No.					

## MANIPAL INSTITUTE OF TECHNOLOGY, MANIPAL 576104

(Constituent College of Manipal University)



TIME: 3 HOURS 30/ 06/2016 MAX. MARKS: 50

## **Instructions to candidates**

प्रज्ञानं ब्रह्म

- Answer **ALL** questions.
- Missing data, if any, may be suitably assumed.
- 1A. Explain indirect addressing modes used in 8086 assembly language programming with suitable example.
- 1B. Justify the need for cache memory. Illustrate direct mapping and fully associative mapping techniques of cache memory management.
- 1C. Draw the functional pin diagram of 8086 microprocessor.

[5+3+2]

- 2A. Write 8086 assembly language program to sort an array of ten decimal numbers in ascending order using selection sort method.
- 2B. With a neat flow chart depict a 3 x 3 unsigned multiplier using *add and shift* method and perform multiplication of multiplicand  $(4)_{10}$  with the multiplier  $(5)_{10}$ .
- 2C. Illustrate the carry save addition process of four 3 bit numbers using block diagram and hardware schematic. [5+3+2]
- 3A. Discuss the format for 8254 software programmable timer/counter IC control word and exemplify the read back feature.
- 3B. Explain the programmed I/O and interrupt I/O methods of transferring data between the computer and a physical I/O device.
- 3C. Write a macro to accept a character string from a user using buffered input function of DOS interrupt. [5+3+2]
- 4A. Explain the following instructions of 8086 microprocessor with one example for each.
  - i. PUSHF

iii. DAS

v. LOOP

ii. XLAT

iv. RCR

- 4B. Write an assembly language program to generate a 40 kHz continuous pulses using counter 1 of 8254 software programmable timer/counter IC.
- 4C. Explain the following 8086 instructions with suitable example

i. SCASB

ii. STOSB

[5+3+2]

- 5A. Draw the internal block diagram of 8255 PPI and summarize the different modes in which the ports of 8255 can be initialized.
- 5B. Perform the division of  $(18)_{10}$  by  $(3)_{10}$  using restoring method. Show all iterative steps involved.
- 5C. Write register transfer logic for 4 x 4 Booth's multiplier used in hardwired design approach of control unit. [5+3+2]

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