Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

II SEMESTER M.TECH (EMAL / PESC) END SEMESTER EXAMINATIONS, MAY 2016

SUBJECT: EMBEDDED SYSTEM DESIGN [ELE 538]

(PROGRAM ELECTIVE – I)

REVISED CREDIT SYSTEM

Time: 3 Hours 10 MAY 2016 MAX. MARKS: 50

Instructions to Candidates:

- Answer **ANY FIVE FULL** questions.
- Missing data may be suitably assumed.
- Support all your programs with relevant comments.

1A. Classify embedded systems based on complexity. Describe them in brief and give relevant examples. ***03***

1B. Explain the following instructions of 8086. Illustrate with an example

i. DIV CX

ii. OR AX, E087H

iii. OUT 84H, AL

iv. WAIT ***04***

1C. Internal marks scored by '07' students in Embedded system design subject is stored in successive memory locations starting at C0050H in extra segment. Write an 8086 ALP to check whether any student has scored full marks (maximum marks: 50). If no student has scored full marks, store 00H in BL register; if at least one student has scored full marks, store FFH in BL register. Use relevant string manipulation instruction of 8086. ***03***

2A. List the salient features of PIC16f877 microcontroller and compare it with Intel 8051 microcontroller ***03***

2B. Describe the limitations of using clock frequency or number of instructions executed per unit time to compare (measure) the processing power of different processors and hence describe how Dhrystone benchmark is useful in this regard. ***03***

2C. Describe the following in brief with respect to memory devices.

i. Write ability and storage permanence

ii. NVRAM

iii. DDRSDRAM

iv. EPROM ***04***

3A. Explain the various compare and test instructions of ARM7TDMI processor. Comment on flag modification in case of all these instructions and illustrate with an example. ***04***

3B. In an energy meter, voltage and current values are sampled at the rate of 250 samples per second (5 samples per cycle). The voltage values for the first cycle are stored in successive locations starting at 0X00008050 and current values are stored starting at 0X00009050. Write an ARM7 ALP with relevant comments to compute average (active) power consumed during the first cycle, using the relation $\frac{\sum_{n=1}^{5} (v(n) * i(n))}{5}$. Assume individual voltage and current values to be 16 bit values and assume the product summation to be within 32 bits. Store the result in 0X00009060 - 0X00009063 (quotient) and 0X00009064 - 0X00009067(remainder). ***04***

3C. Write (single) ARM7TDMI instructions to perform the following operations

i. Subtract 32 bit data in R5 register along with previous carry from 32 bit data in R6 register only if the carry flag is cleared, store the result in R7 register and modify the flags based on the result.

ii. (Assume R0 register to contain (pointing to) 0X00005060) Store R5 register value in 0X0000506C – 0X0000506F, R3 register value in 0X00005068 – 0X0000506B and R1 register value in 0X00005064 – 0X00005067. At the end instruction execution 'R0' register should point to 0X0000506C ***02***

4A. Write a note on non-nested (leaf) and nested subroutines. Describe the instruction of ARM7TDMI used to return from leaf subroutines. With an example, discuss what happens if this instruction is used to return from all subroutines, in case of nested subroutines. Describe a method to overcome this and to return correctly to the calling program. ***03***

4B. Explain the default state of ARM7TDMI when the processor is reset (when Reset exception occurs). Discuss the usual operations (initialization and other operations) to be done inside the reset exception handler.

Write ARM7TDMI instructions to enable IRQ and FIQ interrupts. ***04***

4C. Compare write through and write back techniques with respect to cache memory in case of write hit. Discuss the current trends and developments with respect to cache memory in general purpose and embedded systems. ***03***

5A. Describe the handshake protocol for read operation with respect to parallel communication. Compare it with strobe protocol and list the merits and demerits ***02***

5B. Explain the PCI bus protocol with the help of relevant timing diagram with respect to memory read operation. Assume '4', '16' bit data transferred in the data phase; Target requests for two wait cycles during first data, initiator requests for one wait cycle during third data and no wait cycles during second and fourth data. Clearly explain the functions of all the signals involved in the data transfer. ***05***

5C. Write a 'C' program for PIC16f877 microcontroller to configure MSSP in SPI master mode, transmit data 3BH and 4CH to a slave device and store the received data bytes. Use 250kbps baud rate, idle state for clock as low level, data output at falling edge of clock, sample input data at the end of data output time. Assume fosc = 16MHz and RD5 pin is used to select the slave device. ***03***

6A. Explain the following with respect to USB protocol

i. Connection of devices (tiered star topology). Draw the relevant diagram.

ii. Enumeration (configuration) process.

iii. Bandwidths (data transfer rates) supported. ***04***

6B. Describe the following with respect to Bluetooth wireless communication protocol.

i. Frequency band used for data transfer and number of channels.

ii. Piconet and scatternet.

iii. Active, parked and stand by modes in a piconet. ***04***

6C. What is a watchdog timer? What are the uses of watchdog timer? Describe the working of watchdog timer of PIC16f877. ***02***