Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

SECOND SEMESTER M. Tech (ME/DEAC) E & C DEGREE END SEMESTER EXAMINATION (MAY/JUNE 2016)
SUBJECT: VLSI PHYSICAL DESIGN AND VERIFICATION (ECE - 556)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. Formulate the Integer Linear Programming (ILP) for the case of rigid modules when rotation is not allowed. The dimension of four modules are given as (width (W), height (H)): m_1 (4, 5), m_2 (3, 7), m_3 (6, 4), and m_4 (7, 7). Assume the width (W) is fixed, and possible objective is to minimize the height (H) of the floorplan.

1B. What is a macro cell and how does it function? Realize a multilevel PAL design for the following function f = A'BC + A'B'C' + ABC' + AB'C where 2, 2, 2 wide OR plane is provided for realization.

1C. Consider a Gated Clock implementation where the clock to various logical modules can be individually turned off as shown in **Fig. 1C**. (i.e., Enable1,..., Enable N can take on different values on a cycle by cycle basis). Explain, which approach (A or B) results in lower jitter at the output of the input clock driver?

(5+3+2)

2A. What are the routing quality metrics that should be taken care during placement? For a given placement (P) of blocks a, b, c, d, e and f as shown below in **Fig. 2A** having net $N_1 = (a_1, b_1, d_2)$ with weight w $(N_1) = 2$, net $N_2 = (c_1, d_1, f_1)$ with w $(N_2) = 4$ and net $N_3 = (e_1, f_2)$ with w $(N_3) = 1$. Estimate the total weighted wirelength of P using the RMST and RSMT model.

2B. Explain equipotential and functionally equivalent pins? Perform the nine zone method to do the pin assignment for the pin class M to block A, B, C, D, E, F, G, H and I for the below given **Fig. 2B.**

2C. What is doglegging and how it is advantageous in channel routing? Apply it for Fig. 2C.

(4+4+2)

3A. What is static timing analysis (STA)? Write the top level design flow of Prime Time tool of the Synopsys for Static Timing Analysis (STA)? How tool perform path grouping to generate the prime time reports?

3B. Consider the following programmable I/O block as shown in **Fig. 3B**. Highlight the connection to configure this I/O block as an OUTPUT pin. Specify the five configuration bits and the value of T?

3C. Explain the following terms, design verification, validation and testing?

(5+2+3)

4A. Derive an expression using exact Zero Skew Algorithm (ZSA) for the given **Fig. 4A** (π model of RC network is used here) to get the tapping point position (indicate in figure) and elongated wire length l' for the cases x = 0, x < 1 and x > 1. Here T1, T2 are two sub trees and t1, t2 are the delay between the nodes and leaves, α is the resistance per unit length, β is the capacitance per unit length.

4B. Briefly explain formal verification method using the block diagram?

(6+4)

5A. Estimate the minimum delay of the path from A to B in **Fig. 5A** and choose transistor sizes to achieve this delay. The initial NAND2 gate may present a load of 8 λ of transistor width on the input and the output load is equivalent to 45 λ of transistor width. Also annotate the dotted path given in problem with transistor sizes?

5B. For the given problem in **Fig. 5B**, a relation of gate delays of 3 gates A, B and C has been shown with load capacitance in bar chart. If the input capacitance of buffer y be 0.5fF, 1fF and 1fF with sizes A, B and C respectively. Determine the best size for buffer y that minimizes the actual arrival time (AAT) of sink c.

5C. Briefly explain the need of temporal logic in verification.

(5+3+2)

6A. Briefly explain the event driven simulators? How the timing wheel or event manager managed them? Perform event driven simulation on the following **Fig. 6A** and also draw the timing diagram of the entire events? Assume each gate is having a delay of one unit and no wire delays.

6B. Write the pseudo code for unconstrained Left Edge Algorithm (LEA).

6C. What is minimum clock period of the circuit as shown in **Fig. 6C**?

(5+3+2)

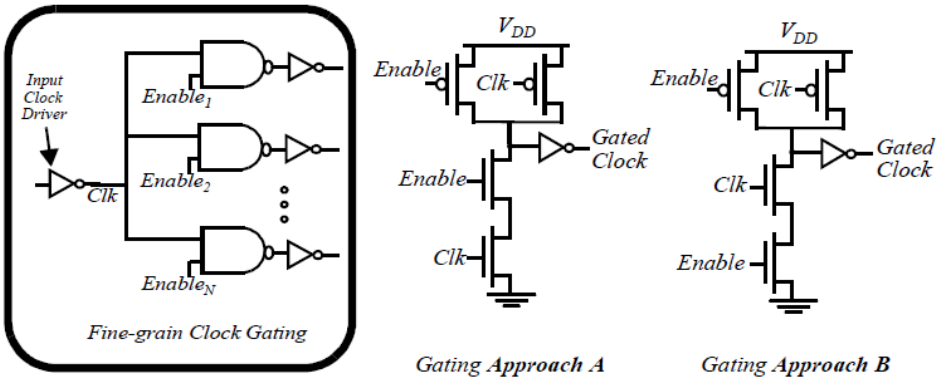


Figure 1C

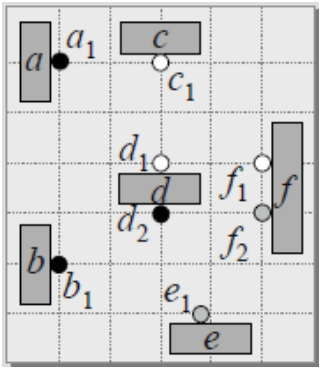


Figure 2A

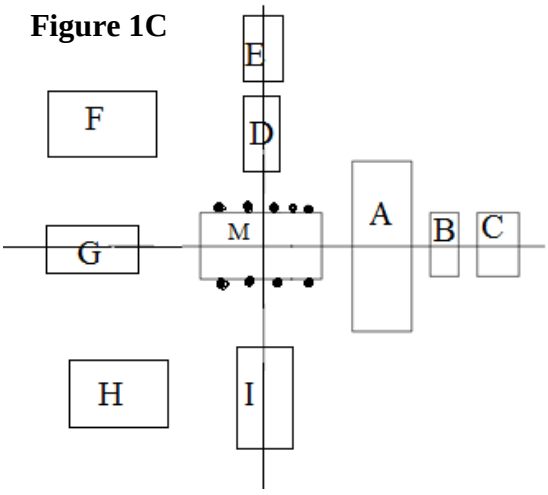


Figure 2B

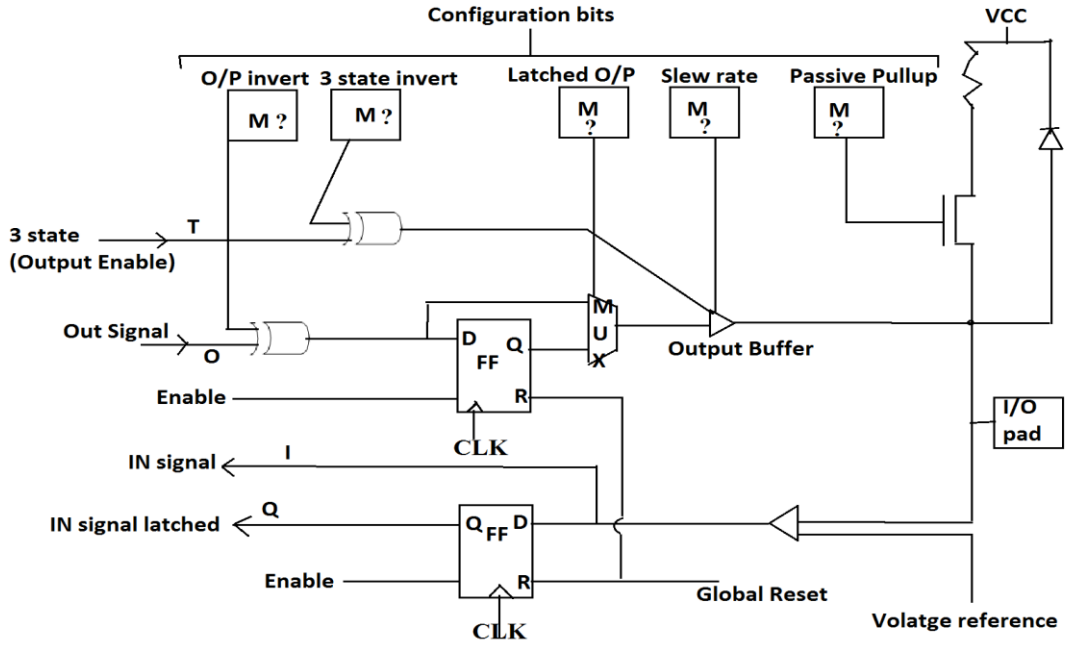


Figure 3B

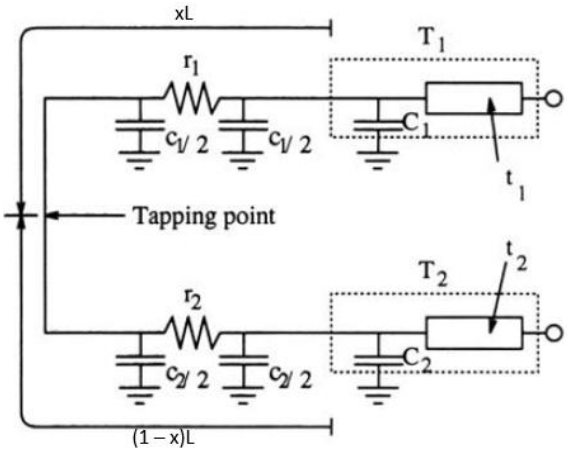


Figure 4A

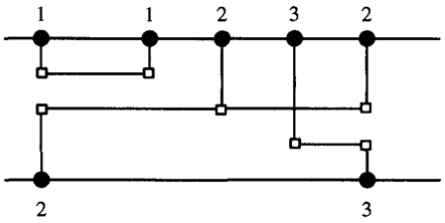


Figure 2C

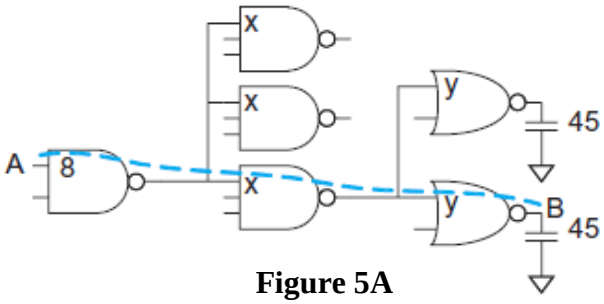
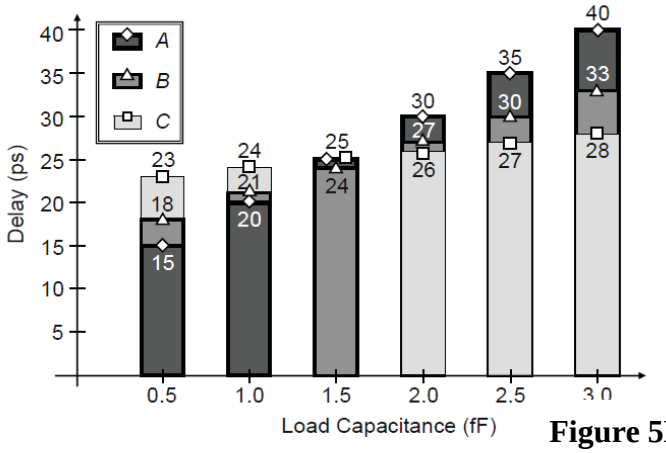


Figure 5A



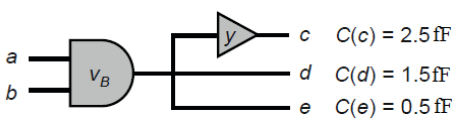


Figure 5B

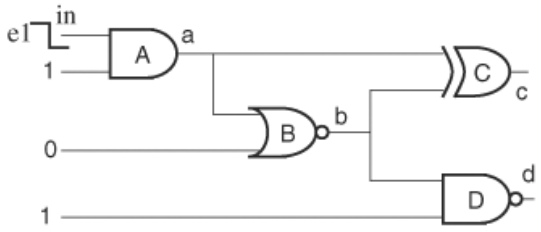


Figure 6A

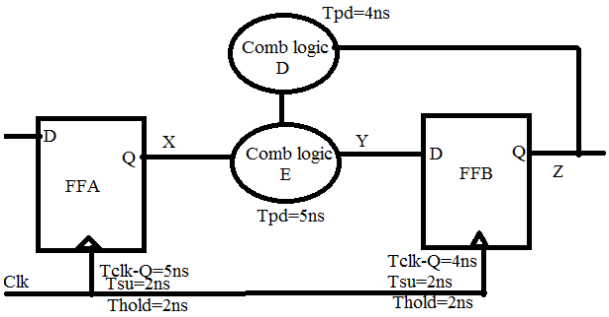


Figure 6C