Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

SECOND SEMESTER M.TECH (ME) DEGREE END SEMESTER EXAMINATION
MAY/JUNE - 2016
SUBJECT: LOW POWER VLSI DESIGN (ECE - 522)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. Explain the following: i) Motivation for Low power VLSI Design
ii) Power aware design Vs. Low power Design.

1B. It is required to design a board for a processor based system consisting of a processor, programmable peripherals, memory (both RAM & ROM) and I/O controllers. Identify the regions and places where you can apply the low power techniques. List the techniques and justify your selection and suitability.

(5+5)

2A. Explain the following with the help of suitable diagram:

i) Guarded Evaluation
ii) Clock Gating
ii) Pre-computation

2B. With suitable illustrations, explain Dynamic Supply Gating technique for low power operation.

(6+4)

3A. Explain Dual V_{DD} technique in VLSI circuits to reduce dynamic power and list the merits and demerits.

3B. The circuit shown in **Figure. 3B,** is designed in 65nm CMOS technology using low threshold transistors. Each gate has a delay of 6ps and a leakage current of 10nA. Given that a gate with high threshold transistors has a delay of 12ps and leakage of 1nA, optimally design the circuit with dual-threshold gates to minimize the leakage current without increasing the critical path delay. What is the percentage reduction in leakage power? What will the leakage power reduction be if a 30% increase in the critical path delay is allowed?

(5+5)

4A. Describe subthreshold leakage in MOSFETs and explain any TWO techniques for reducing the same.

4B. What is the impact of using repeaters in in interconnects? Explain. Also explain the demerits of using repeaters.

4C. List the main leakage sources in MOSFETs.

(5+3+2)

5A. Explain different DPM policies and compare them.

5B. Explain the basic principle of adiabatic switching and its applicability in VLSI circuits.

5C. List the device level modifications for low power applications.

(5+3+2)

6A. Explain with illustrations and examples low power opportunities available in memory and processor memory interface.

6B. Explain with examples the key techniques used while coding so as to reduce power dissipation.

6C. Explain the significance of procrastination scheduling for low power.

(5+3+2)

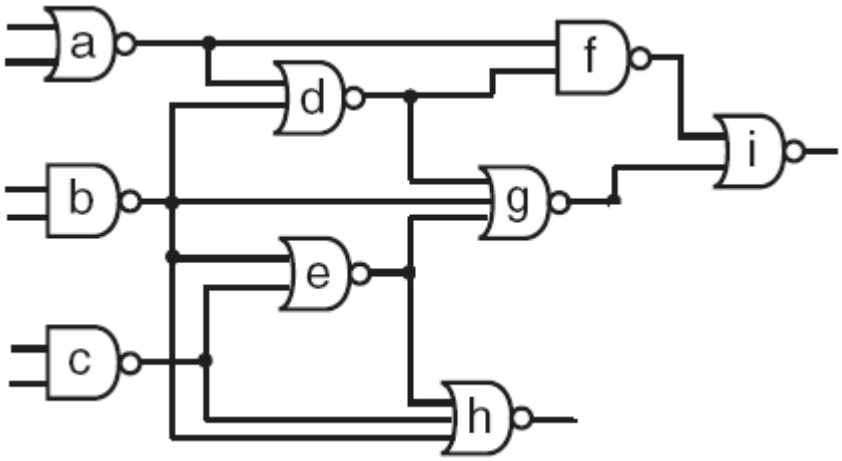

Figure. 3B