Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

SECOND SEMESTER M. Tech (ME/DEAC) DEGREE END SEMESTER EXAMINATION
MAY/JUNE 2016
SUBJECT: VLSI PHYSICAL DESIGN AND VERIFICATION (ECE - 556)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. Briefly explain each design stage of Analog design flow? What is the meaning of back annotating a design?

1B. Explain zero cycle path with timing diagram? Which timing violation will be in these paths?

1C. Classify Programmable ASIC? What is the difference between CPLD and FPGA?

(5+3+2)

2A. Why is it necessary to check the critical path of a design? Find the critical path (and highlight it) in the half adder circuit as shown in FIG. 2A and check through path sensitization whether it is a true or false path, if it's true find the test vectors. Assume no wire delay and the gate delays are given in table of FIG. 2A.

2B. What are wire load models? Explain the synopsis wire load modes associated with the command "set_wire_load_mode"?

2C. A netlist is represented by two vectors TOP = [A B A 0 E D 0 F] and BOT = [B C D A C F E 0] with pin connections ordered from left to right.
(a) Find S (col) for 8 columns a, b, c, d, e, f, g, h and the minimum number of routing tracks.
(b) Draw the HCG and VCG.

(4+3+3)

3A. Briefly explain the cycle based simulators? Do the levelization and apply the topological sort using Depth First Search (DFS) algorithm for the FIG. 3A to get the proper evaluation order?

3B. Briefly explain the design challenges in verification by taking the appropriate example of your choice.

3C. Find the best and worst case rising and falling output transition of 3-input NAND gate driving h identical 3-input NAND gate using Elmore delay model. Transistor widths are chosen to achieve effective rise and fall time and pull-down resistance equal to that of a unit inverter (R).

(4+3+3)

4A. Briefly explain the IR drop, Ldi/dt and electro-migration effect and remedy to resolve these issues during design of power distribution network. In the given FIG. 4A, Which approach is better for power distribution?

4B. What is the objective of pin assignment? Perform the method of topological pin assignment between the main component 'm' to an external block 'b' as shown in FIG. 4B.

4C. Write the difference between floorplan and placement? For a given placement as shown in FIG. 4C, the following nets N1 (A, B), N2 (E1, F1), N3 (A, D1, G), N4 (C, D2), N5 (E2, F2, D3), find the wire density and check whether the placement is routable or not? Assuming that the capacity of each edge is 3 tracks and the weight of each net to be unity, here h1, h2, h3, h4, h5, h6 corresponds to local horizontal cut and v1, v2, v3, v4, v5, v6 corresponds to local vertical cut.

(5+2.5+2.5)

5A. Briefly explain the use of Binary Decision Diagram (BDD) in formal property based verification (FPV)? For the BDD in FIG. 5A, do the following:

a) Remove the redundancy and obtain a canonical Ordered Binary Decision Diagram (OBDD).
b) Derive the function of the obtained OBDD in step (a) in sum-of-products form.
c) Repeat (b) for product of sums.

5B. Apply the exact Zero Skew Algorithm (ZSA) to find the final point of clock source to connect the four sinks points located at A(8, 0) with capacitance (C') = 16 Farad, B(22, 6) with C' = 10 Farad, C(0, 10) with C' = 1 Farad and D(5, 15) with C'= 2 Farad as shown in FIG. 5B. Grow the clock network in a fashion (A, B) and (C, D) and highlight the connection from source to sinks (A, B, C, D) with proper diagram. Assume resistance per unit length $\alpha = 0.1\ \Omega$ and capacitance per unit length is $\beta = 0.2$ Farad.

(5+5)

6A. Given the following netlists with six cells [C1, C2, C3, C4, C5, C6] and six nets N1 = {C1, C3, C4, C6}, N2 = {C1, C3, C5}, N3 = {C1, C2, C5}, N4 = {C1, C2, C4, C5}, N5 = {C2, C5, C6} and N6 = {C3, C6}. Apply the Linear Ordering Algorithm (LOA) to find the order of blocks to grow the floorplan? Assume C1 as seed block.

6B. Explain the basic principle of design verification? Consider the specification of two way arbiter having following signals r1, r2 request lines, g1, g2 are grant lines, and clk. Some properties of the arbiter are given as,

1. Either g1 or g2 is always false (mutual exclusion)
2. Whenever r1 is asserted, g1 is given in the next cycle.
3. When r2 is the sole request, g2 comes in the next cycle.
4. When none are requesting, the arbiter parks the grant on g2.

Now if an RTL designer has the implementation as in FIG. 6B, do the property checking.

(5+5)

Gate	Intrinsic delay
AND	3 ns
OR	2 ns
XOR	5 ns

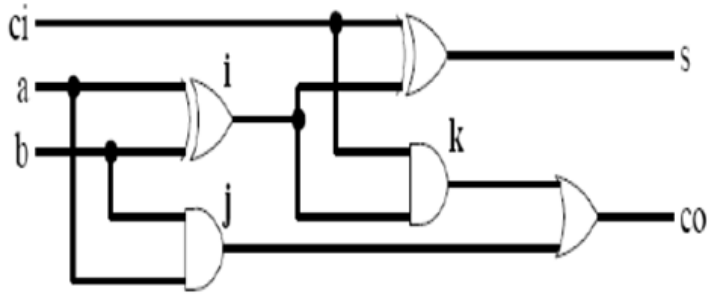

FIG 2A

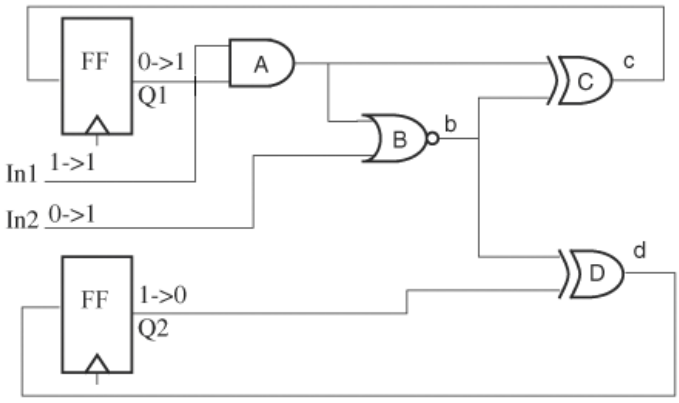

FIG 3A

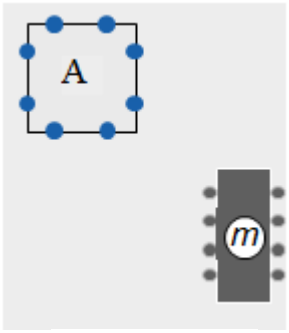

FIG 4B

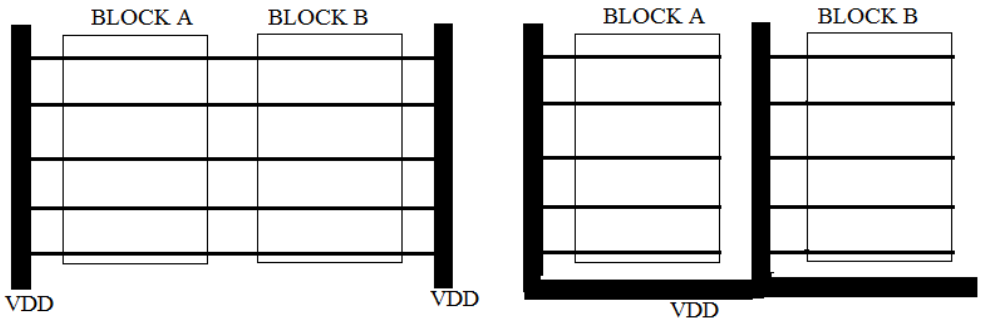

FIG 4A

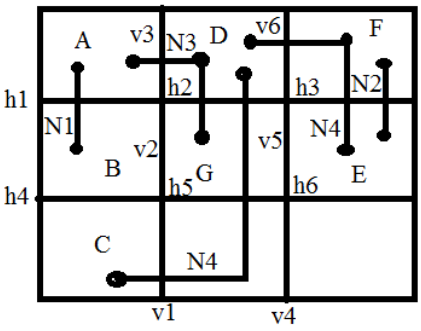

FIG 4C

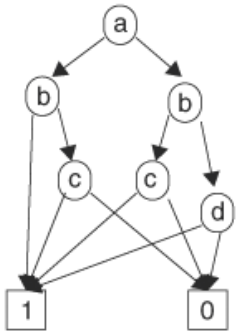

FIG 5A

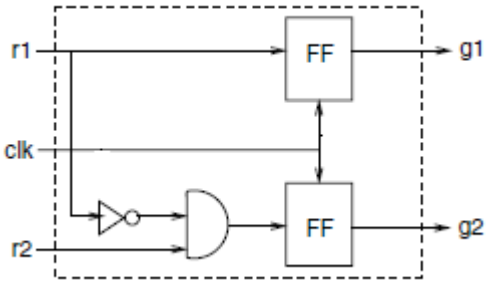

FIG 6B

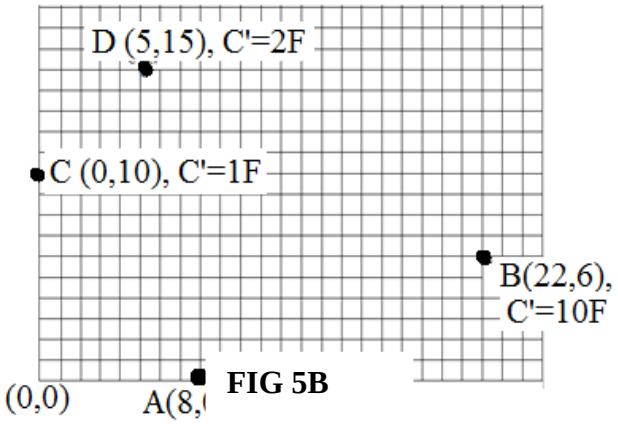

FIG 5B