Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

SECOND SEMESTER M.TECH (ME) DEGREE END SEMESTER EXAMINATION
MAY / JUNE 2016
SUBJECT: VLSI TESTING & TESTABILITY (ECE - 553)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. Consider the ISCAS 87 circuit as shown in **Figure 1A**. Find Test vector for Multiple fault at net-list 11 and 19 (both at SA0) using BDD. Draw ROBDD and ITE of the circuit also.

1B. Explain in detail different modes of operation of BILBO.

1C. Explain the differential non-linearity in DAC with example.

(5+3+2)

2A. For the circuit shown in **Figure 2A**

(i) What is the number of all potential fault sites?
(ii) Derive the equivalence collapsed set. What is the collapse ratio?
(iii) Derive the dominance collapsed set. What is the collapse ratio?

2B. Consider the circuit shown in **Figure 2B**. Find the test vector using PODEM algorithm.

2C. Explain the basic principle of IDDQ fault.

(5+3+2)

3A. For the circuit as shown in **Figure 3A**, perform deductive fault simulation to determine all faults that will be detected at the primary output 'o' for the test vector a=1 b=0 c=1.

3B. Given in a **Figure 3B** SCOAP testability measure of a circuit. Find Test vector using FAN algorithm.

3C. Explain the Parallel Board / MCM Scan with neat diagram.

(5+3+2)

4A. Consider the function F (x y z w) = xy'+xyz+yw'+x'yz', draw the ROBDD using reduction rule.

4B. Perform ATPG on the circuit shown in **Figure 4B** using SOCRATES and SCOAP measures to test the fault *h*1 at SA1.

(5+5)

5A. For the circuit shown in **Figure 5A**, the fault α is at SA0, SA1. Find
(i) the Propagating inputs at each level of circuit to observe the fault at Z.
(ii) the minimal set of test vector for observed fault. **Use path sensitization technique.**
(iii) Draw the fault path and find control input condition required for MUX for fault to be observable.

5B. A three input gate BOMB (**Figure 5B (i)**), who's characteristic are shown in **Figure 5B(ii)**, has been mass-produced by an unfortunate Chinese company. Experimental evidence shows that input combination shown below in **Figure 5B (iii)** are responsible to BOMB to explode. The company official has hired "**Sherlock Homes"** to find the cause of it. Sherlock Homes has following tasks to do

(i) to find the possible combinations for which BOMB has exploded.
(ii) to check whether the circuit is completely useless?
(iii) to look whether fault/faults can be identifiable? Use any fault detection technique.

(5+5)

6A. Consider the circuit shown in **Figure 6A** with 'a' is at SA1 and 'b' is at SA0. **Use Boolean difference technique** to find (i) Z, Z_a and Z_b. (ii) check if (101) detects Z_a (iii) check if (101) distinguishes Z_a & Z_b.

6B. Find the Test vector of sequential circuit using Time Frame expansion method for the circuit shown in **Figure 6B**.

(5+5)

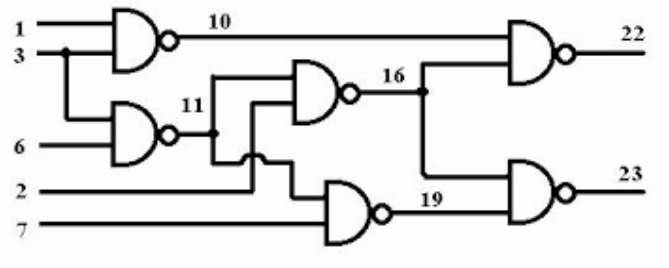


Figure 1A

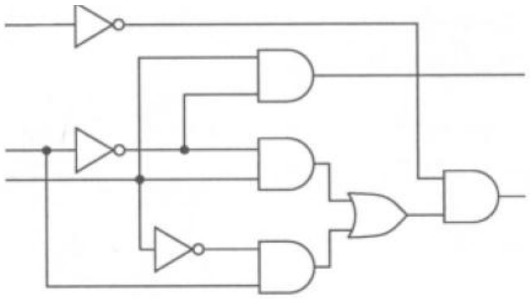


Figure 2A

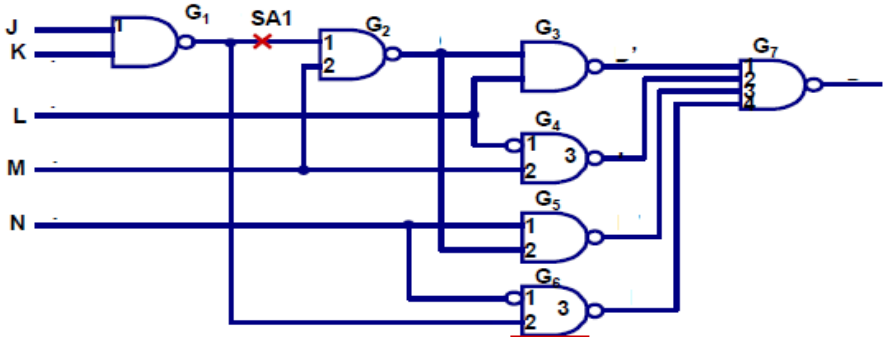


Figure 2B.

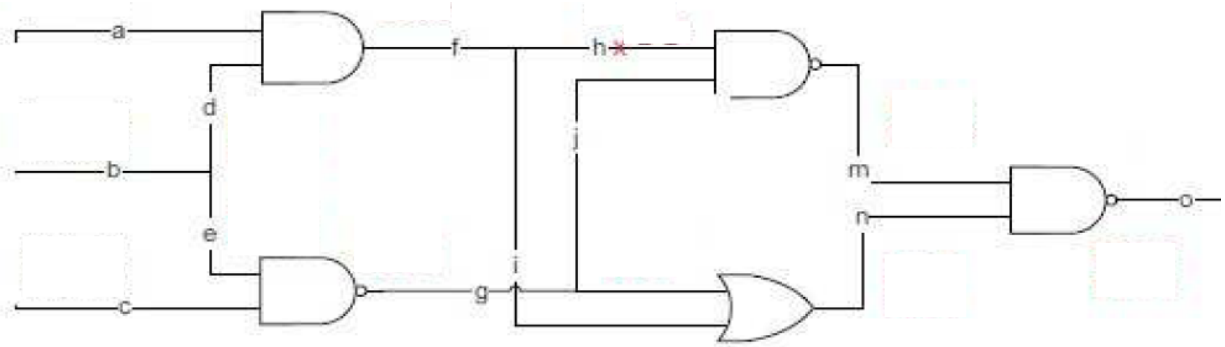


Figure 3A.

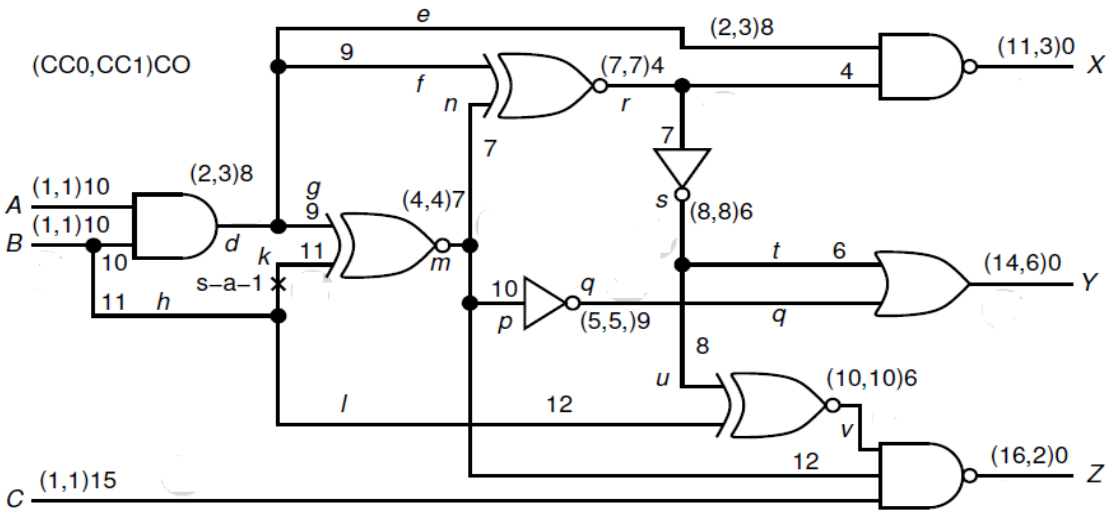


Figure 3B.

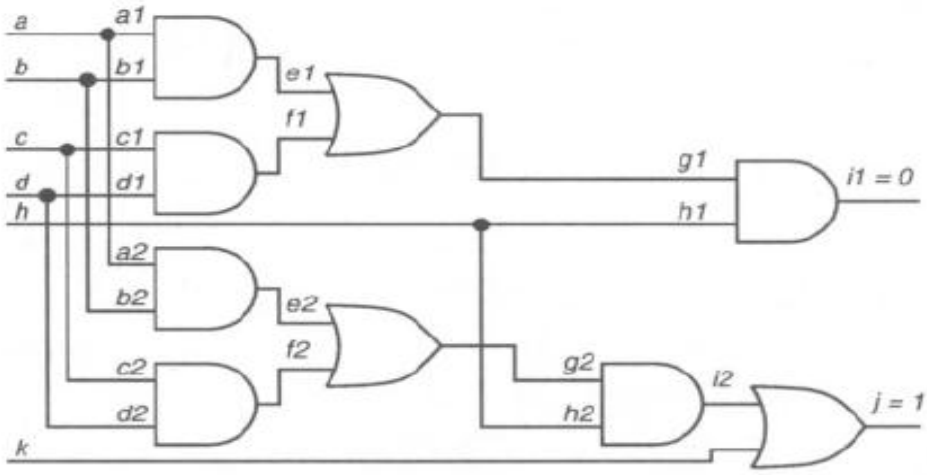


Figure 4B

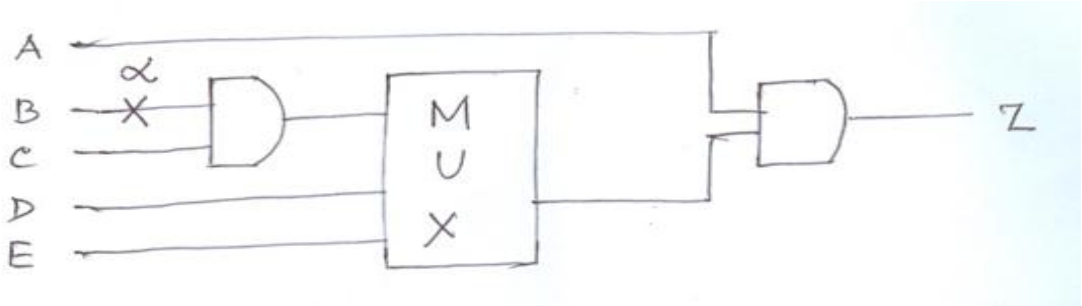
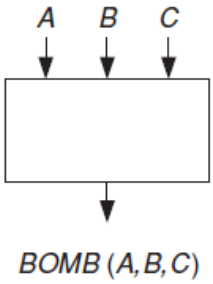


Figure 5A



C \ AB	00	01	11	10
0	1	1	0	1
1	0	1	0	0

BOMB (A,B,C)

C \ AB	00	01	11	10
0	1	0	0	1
1	0	0	1	1

BOMB (A,B,C)

Figure 5B (i) Combination **Figure 5B (ii) Correct Combination** **Figure 5B (iii) Wrong**

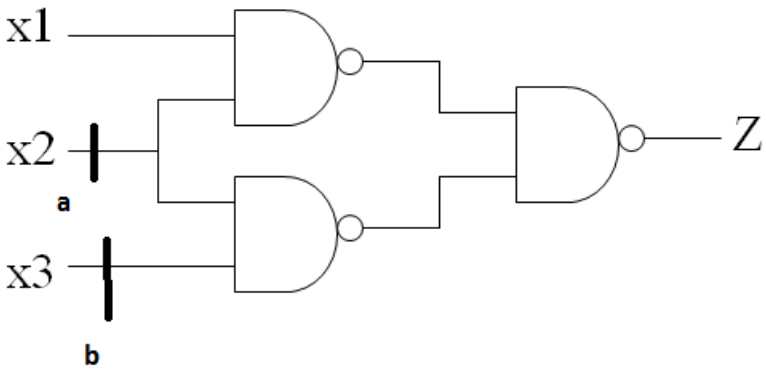


Figure 6A.

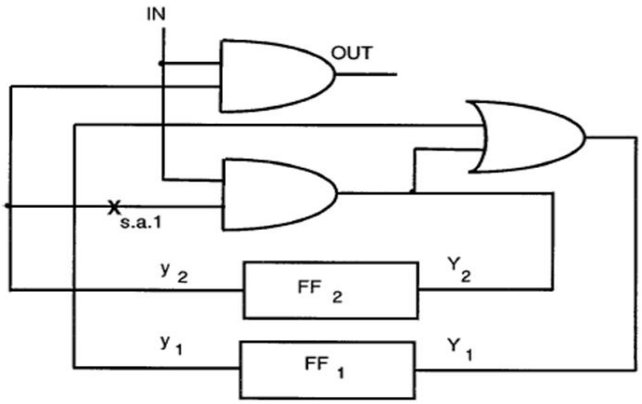


Figure 6B