| Reg. No. | | | | | | | | | | |
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MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

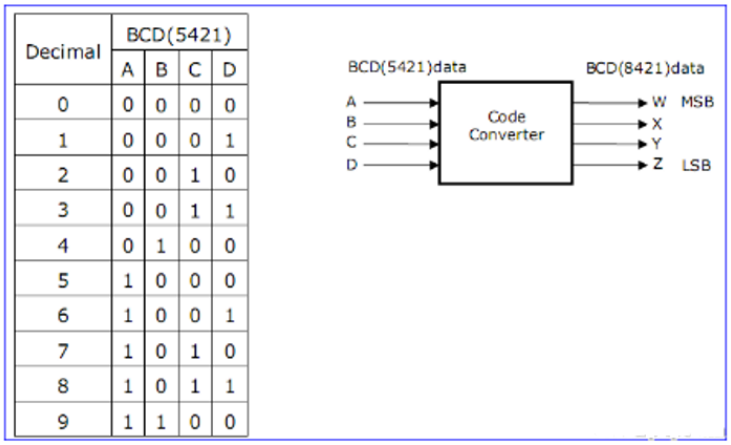
**FIRST SEMESTER M.Tech. (INDUSTRIAL AUTOMATION AND ROBOTICS) DEGREE END SEMESTER EXAMINATION**
**November /December 2016**
**SUBJECT: ANALOG AND DIGITAL ELECTRONICS (MTE-5131)**

**TIME: 3 HOURS** **MAX. MARKS: 50**

**Instructions to candidates**
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

| | | |
|---|---|---|
| 1A. | Servokon systems has recruited you as a design engineer. Your first task is to design a circuit for a voltage stabilizer that clamps the input waveform by 5 V. Design the circuit using an op-amp with necessary waveforms to support your design. | (7) |
| 1B. | Give a short note on the design of an Integrator using an op-amp. Support your answer with suitable equations. | (3) |
| | | |
| 2A. | Differentiate between low pass and high pass active filters with suitable circuit diagrams. | (3) |
| 2B. | Velodynelidar is a manufacturer of LiDAR equipment used in scanners and sensors. Suggest the design of a filter that passes green color light only in the range of 520-560 nm. | (7) |
| | | |
| 3A. | According to the system shown in Fig. 3 A below, design a 5421 to 8421 code converter. | (5) |
| 3B. | The operating conditions (ON = 1 and OFF = 0) of three pumps (x, y, z) are to be monitored. x = 1 implies that pump x is ON, and so is the case for pumps y and z. It is required that the indicator LED, P shown in Fig. 3 B below, should glow if majority of the pumps fail. Enter the logical values in the K-map in the format shown in Fig. 3 B, and derive the SOP expression, whose output is logical value 1, when a majority of the pumps fail. | (5) |
| | | |
| 4A. | Describe the architecture of the Xilinx 3020 CLB with a suitable circuit diagram. | (5) |
| 4B. | Differentiate between the shareable and parallel expanders used in the ALTERA 7000 series of FPGAs. | (5) |
| | | |
| 5A. | Analyse the Fig 5A and answer the following questions:<br>i. What is the content of DATA register?<br>ii. What would be the output for the instruction accessing DATA [8] [2]?<br>iii. What would be the output for the instruction accessing DATA [8] [6:2]? | (3) |
| 5B. | Write a Verilog program to perform the gate level modelling of the circuit shown in Fig 5 B. | (7) |
| | | |
| 6A. | Analyse the sequential circuit shown in Fig 6 A. | (5) |

| | |
|---|---|
| 6B. | Design a sequential circuit using D flip flops for a lift that operates for two floors, GROUND and FIRST. When the UP button is pressed, the lift goes from GROUND to FIRST floor and a RED LED glows. When the DOWN button is pressed, the lift goes from FIRST to GROUND floor and a GREEN LED glows. Arrive at the final circuit by first designing the finite state machine (state diagram). (5) |
| | |



| Decimal | BCD(5421) | | | |
|---|---|---|---|---|
| | A | B | C | D |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 1 | 0 | 0 | 0 |
| 6 | 1 | 0 | 0 | 1 |
| 7 | 1 | 0 | 1 | 0 |
| 8 | 1 | 0 | 1 | 1 |
| 9 | 1 | 1 | 0 | 0 |



Figure 3A

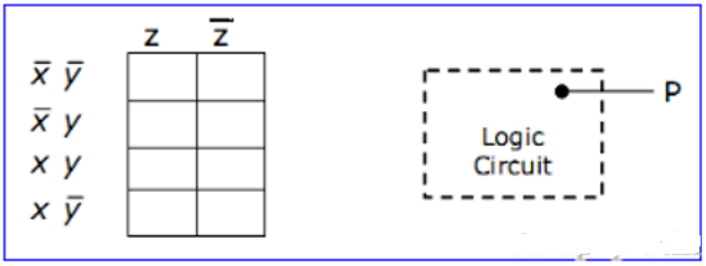




Figure 3B

Verilog Code:

```
reg [8:1] DATA;
reg DRAM [10:1];
DATA = DRAM [8];
```

DRAM Memory:

| |
|---|
| 10101010 |
| 11011010 |
| 11111111 |
| 00000000 |
| 11110000 |
| 00001111 |
| 01010101 |
| 11001100 |
| 00110011 |
| 00011100 |

Figure 5A

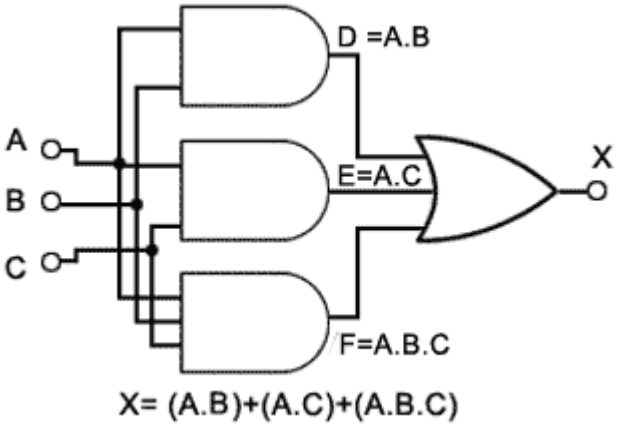



Figure 5B

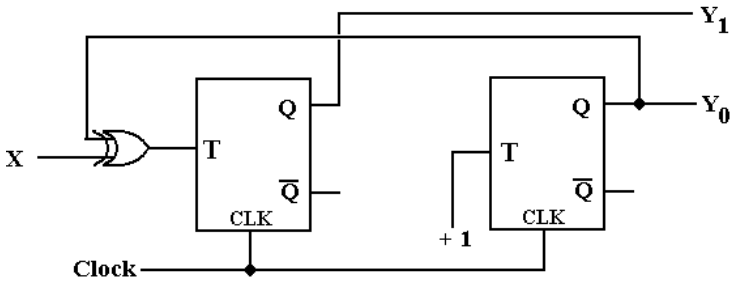



Figure 6A