Reg. No.									

MANIPAL UNIVERSITY
SCHOOL OF INFORMATION SCIENCES

MASTER OF ENGIEERING – ME FIRST SEMESTER (VLSI DESIGN / SECOND SEMESTER EMBEDDED SYSTEMS) DEGREE EXAMINATION – APRIL / MAY 2016

SUBJECT: EDA 611 / ESD 616.1(ELECTIVE - 2) – HIGH LEVEL DIGITAL DESIGN

Wednesday, April 27, 2016

Time: 10.00 – 13.00 Hrs. Max. Marks: 100

1. Implement the F = ∑XYZ (1, 2, 5,7) logic function using multiplexer. (10 marks)
2. Design a digital circuit to count the following sequence. (10 marks)
   0, 1, 2, 3, 2, 3, 0, ...
3. Design a 1101 sequence detector using Mealy Machine. (10 marks)
4. Design the 8 bit barrel shifter which can perform3 bit right shift and 4 bit leftshift. (10 marks)
5. Explain the tree adder, Brent-Kung Adder. (10 marks)
6. Define the following, (2x5 = 10 marks)
   a) Setup time
   b) Hold time
   c) False path
   d) Multi cycle path
   e) Clock skew
7. Design a dual port asynchronous memory with neat diagram. (10 marks)
8. Explain EAB structure in Altera FPGA. (10 marks)
9. Briefly explain the Burst & Wrap Operation. (10 marks)
10. Design Real Time Clock with following features, (10 marks)
    a) Display – Hr : Min : Sec
    b) Clock freq 400 KHz

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