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MANIPAL UNIVERSITY SCHOOL OF INFORMATION SCIENCES

SECOND SEMESTER MASTER OF ENGINEERING – ME (VLSI DESIGN)
DEGREE EXAMINATION (MAKE-UP) – JULY 2016

SUBJECT: EDA 604 - ADVANCED VLSI DESIGN

Saturday, July 9, 2016

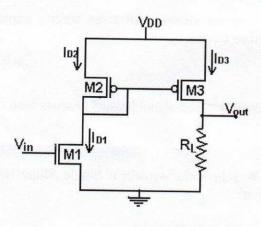
Time: 10.00 – 13.00 Hrs.

Max. Marks: 100

 Starting from a general 2-port network, derive a complete low frequency, small signal model for a MOSFET.

(10 marks)

2. A) With relevant diagrams, differentiate among current source, current sink and current mirror. B) Calculate the small-signal voltage gain of the circuit shown in Fig. 2(B).



(5+5=10 marks)

3. With a neat schematic diagram, explain the working of Wilson current mirror. How it is different from a simple cascode current mirror?

Figure 2(B)

(10 marks)

4. Derive the expression for the small-signal incremental voltage gain, A_v of a CMOS Common-Source amplifier with diode-connected load. What are the merits and demerits of this topology over the passive load connected one?

(10 marks)

- 5. A) What are the characteristics of an ideal current or voltage references?
 - B) Design a 3V reference using MOSFET-Only voltage divider. Determine the temperature coefficient of the reference. Assume any missing data.

[Data given: $V_{DD} = +5V$, $V_{SS} = 0V$, $V_{THN} = 0.8V$, $V_{THP} = 0.9V$, $\partial V_{THN}/\partial T = -0.0024V/C$, $\partial V_{THP}/\partial T = -0.0027V/C$]

(5+5=10 marks)

- 6. What is differential amplification? What are its advantages over single-ended amplification? (10 marks)
- What is Common Mode Rejection Ratio (CMRR) of a differential amplifier? Explain the diagram used to measure it.
 (10 marks)
- 8. With a neat schematic diagram showing all three stages, explain the working of a CMOS , nonlinear analog comparator circuit. (10 marks)
- 9. What are the issues involved in mixed-signal layout? Discuss each of them briefly. (10 marks)
- 10. With the help of a block schematic, explain a Single Slope Integrating ADC. What are the accuracy issues related to it?
 (10 marks)
