Reg. No.										

MANIPAL UNIVERSITY
SCHOOL OF INFORMATION SCIENCES

SECOND SEMESTER MASTER OF ENGINEERING - **ME** (VLSI DESIGN)
DEGREE EXAMINATION (MAKE-UP) – JULY 2016

SUBJECT: **EDA 612 - SCRIPTING FOR VLSI**

Monday, July 11, 2016

Time: 10.00 – 13.00 Hrs. Max. Marks: 100

1. What is Shell? Why use Shell? List and explain different types of shell. (10 marks)

2. Discuss the following in Linux
   a. Boot Block, Super Block, Inode Table, Data Block (4 marks)
   b. df, dfspace, du, ulimit (6 marks)

3. With an example, discuss the following Linux utilities. (5x2=10 marks)
   a. Sort b. uniq c. comp d. head e. tail

4. With an example, explain test command for unary file operator (10 marks)

5. With respect Perl, discuss the following with an example (5x2=10 marks)
   a. Shift b. unshift c. push d. pop e. splice

6. Explain with an example wrt to Perl (2x5=10 marks)
   a. Arithmetic operator
   b. Relational Operator

7. With respect to Perl, discuss the following regular expression with an example (3 + 3 + 4 =10 marks)
   a. Binding Operators
   b. Character Class
   c. Grouping

8. Explain references, dereferences, circular reference with an example wrt to Perl (10 marks)

9. Explain the File I/O with an example (10 marks)

10. Write a Perl script to extract all cell name from the given timing report (10 marks)
(**Example:** buf1a27 → Buffer)

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Startpoint: FF1 (rising edge-triggered flip-flop clocked by Clk)
Endpoint: FF2 (rising edge-triggered flip-flop clocked by Clk)
Path Group: Clk
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock Clk (rise edge)                    0.00       0.00
clock network delay (propagated)         1.10 *     1.10
FF1/CLK (fdef1a15)                       0.00       1.10 r
FF1/Q (fdef1a15)                         0.50 *     1.60 r
U2/Y  (buf1a27)                          0.11 *     1.71 r
U3/Y  (buf1a27)                          0.11 *     1.82 r
FF2/D (fdef1a15)                         0.05 *     1.87 r
data arrival time                                   1.87

clock Clk (rise edge)                    4.00       4.00
clock network delay (propagated)         1.00 *     5.00
FF2/CLK (fdef1a15)                                  5.00 r
library setup time                      -0.21 *     4.79
data required time                                  4.79
-----------------------------------------------------------
data required time                                  4.79
data arrival time                                  -1.87
-----------------------------------------------------------
slack (MET)                                         2.92
```

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