Reg. No.									

MANIPAL UNIVERSITY
SCHOOL OF INFORMATION SCIENCES

SECOND SEMESTER MASTER OF ENGINEERING - **ME** (VLSI DESIGN)
DEGREE EXAMINATION – APRIL / MAY 2016

SUBJECT: EDA 608 – LOW POWER VLSI DESIGN

Saturday, April 30, 2016

Time: 10.00 – 13.00 Hrs. Max. Marks: 100

1. Derive an expression for the short-circuit power dissipation component in a CMOS circuit. Discuss how to reduce short-circuit power.

(10 marks)

2. A battery-operated 65nm digital CMOS device is found to consume equal amounts (P) of dynamic power and leakage power while the short-circuit power is negligible. The energy consumed by a computing task, that takes T seconds, is $2PT$. Compare the below two power reduction strategies for extending the battery life:

   a. Clock frequency is reduced to half, keeping all other parameters constant.
   b. Supply voltage is reduced to half. This slows the gates down and forces the clock frequency to be lowered to half of its original (full voltage) value. Assume that leakage current is held unchanged by modifying the design of transistors.

(10 marks)

3. Explain with diagrams, the following multiple V_{TH} techniques to suppress the sub-threshold leakage current:
   a. Multi-threshold CMOS (MTCMOS)
   b. Dual Threshold CMOS

(5+5 = 10 marks)

4. State and prove a theorem specifying the condition for zero short-circuit power consumption in a CMOS gate.

(10 marks)

5. Write a short note on:
   a. Reliability-Driven Voltage Scaling Approach
   b. Technology-Driven Voltage Scaling Approach

(5+5 = 10 marks)

6. Explain with the help of neat diagrams, Architecture-Driven Voltage Scaling technique by trading area for lower dynamic power through hardware duplication. (10 marks)

7. Explain Gate Triggering Approach to minimize the glitch power with an example. (10 marks)

8. Describe the principle of operation of Adiabatic Power Supply. (10 marks)

9. Explain the most popularly used logic optimization techniques for power reduction. (10 marks)

10. Discuss system design issues with multi-voltage designs. (10 marks)

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