Reg. No.										

MANIPAL UNIVERSITY
SCHOOL OF INFORMATION SCIENCES

SECOND SEMESTER MASTER OF ENGINEERING – **ME** (VLSI DESIGN)
DEGREE EXAMINATION – APRIL / MAY 2016

SUBJECT: EDA 616.8 (ELECTIVE 2) – PHYSICAL DESIGN

Friday, May 6, 2016

Time: 10.00 – 13.00 Hrs. Max. Marks: 100

1. A. Calculate thé peak current and power dissipation of a large ASIC chip operating at 1.8V and 50MHz speed, having 10K registers with capacitance 0.5pF, with a rise/fall time of 1ns.
   B. Write a note on clock distribution

   (5+5 = 10 marks)

2. Explain the procedure involved in a floorplan

   (10 marks)

3. A. What are input, output, goal and challenges of a placement in ASIC design
   B. Explain cluster and region in global placement

   (4+6 = 10 marks)

4. Explain the following.

   A. Slice and bisection placement
   B. Bisection placement

   (5+5 = 10 marks)

5. Explain different types of clock skews with example

   (10 marks)

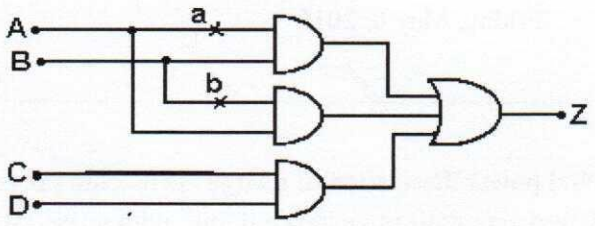
6. Discuss various aspects of detailed routing.

   (10 marks)

7. What are the advantages of modeling physical faults as logical faults? List and briefly explain different types of fault models.

   (10 marks)

8. Find the test vector set to detect a s@0 and b s@1 for the figure shown below.



(10 marks)

9. Explain parallel fault and deductive fault simulation with an example each.

(10 marks)

10. Explain the significance of LFSRs. With a schematic diagram, explain a 4 bit LFSR with 0000 state.

(10 marks)

*****