Reg. No.									

MANIPAL UNIVERSITY
SCHOOL OF INFORMATION SCIENCES

SECOND SEMESTER MASTER OF ENGIEERING – **ME** (VLSI DESIGN) DEGREE EXAMINATION – APRIL / MAY 2016

SUBJECT: EDA 610 - UNIVERSAL VERIFICATION METHODOLOGY

Thursday, April 28, 2016

Time: 10.00 – 13.00 Hrs. Max. Marks: 100

1. Write short notes on (5 + 5 =10 marks)
   a. Transactor (Agent)
   b. Scoreboard

2. Write short notes on the following in SystemVerilog randomization (2 + 2 + 6 = 10 marks)
   a. Rand
   b. Randc
   c. Constraint block

3. Write short notes on the following with example (5 + 5 = 10 marks)
   a. Inheritance
   b. Abstraction

4. Write short note on uvm_component class. (10 marks)

5. Write short note on Integration level environment. (10 marks)

6. Explain Clean up phase in UVM Testbench. (10 marks)

7. Write short notes on UVM Factory coding convention 1 and convention 3 with example. (10 marks)

8. Write short notes on Object Overrides in UVM. (10 marks)

9. Write short notes on UVM sequences and tests with example. (10 marks)

10. Explain different UVM reporting with examples. (10 marks)

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