Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

SIXTH SEMESTER B. Tech. (E & C) DEGREE END SEMESTER EXAMINATION
MAY/JUNE 2016
SUBJECT: ASIC DESIGN (ECE - 320)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Graph sheet will be provided.
- Missing data may be suitably assumed.

1A.	Implement 0101 overlapping sequence detector using PLA. Use minimum hardware.
1B.	Implement the F=a'cd+ b'cd+ab+bc' using ALTERA MAX structure having 3-wide OR Plane
1C.	What is floor plan? Give an example of non-slicing floorplan.
	(5+3+2)
2A.	Given the following netlist with six cells [L, M, N, O, P, Q] and six nets N_1={L, N, O, Q}, N_2={L, N, P}, N_3={L, M, P}, N_4={L, M, O, P}, N_5={M, P, Q} and N_6={N, Q} Find the linear ordering using linear ordering algorithm.
2B.	Sketch a 2-input NOR gate with transistor widths chosen to achieve effective rise and fall resistances equal to a unit size inverter. Compute the rising and falling propagation delays of the NOR gate driving *h* identical NOR gates using the Elmore delay model. Assume that every source or drain has fully contacted diffusion when making your estimate of capacitance.
2C.	A Cell Based ASIC is using AND gate as standard cell and two 2 to 4 decoder as fixed block. Implement a 4 to 16 decoder.
	(5+3+2)
3A.	Perform a single pass of Fiduccia and Mattheyses algorithm on the circuit shown in **FIG. 3A** using *{bcde, afgh}* as the initial solution. Break ties in alphabetical order. The area constraint is set to [3, 5].
3B.	Briefly Explain the ASIC Design flow with neat diagram.
3C.	A ring oscillator is constructed from an odd number of inverters, as shown in **FIG. 3C** Estimate the frequency of an *N*-stage ring oscillator. The logical effort and parasitic delay of the inverter are g = 1 and p=1 respectively. Find the maximum operating frequency of the oscillator.
	(5+3+2)
4A.	Write the Verilog code for 4-bit adder and its test-bench.
4B.	**FIG. 4B** shows the placement *P* of blocks *a-f* and their pins, nets N_1 = ($a1$,$b1$,$d2$), N_2 = ($c1$,$d1$,$f1$) and N_3 = ($e1$,$f2$). The weights of net N_1, N_2, and N_3 are 2, 4 and 1 respectively. Estimate the total weighted wirelength of *P* using the RMST model.
4C.	What is placement?
	(5+3+2)

5A.	Show that the diffusion capacitance of conventional 24 λ / 12 λ CMOS inverter is reduced by 50% after the layout folding. Draw the folded layout. Given that a unit size transistor with width =4 λ offers the diffusion capacitance C.
5B.	Find the equivalence partition and the corresponding reduced machine for the state machine represented by **TABLE 5B.**
5C.	Explain the working of floating gate MOSFET.
	(5+3+2)
6A.	Find the longest path for the DAG graphs shown in **FIG 6A.**
6B.	Write the Verilog test-bench for 3 input OR gate.
6C.	What is logical effort? Find the logical effort of 3-input NAND gate.
	(5+3+2)

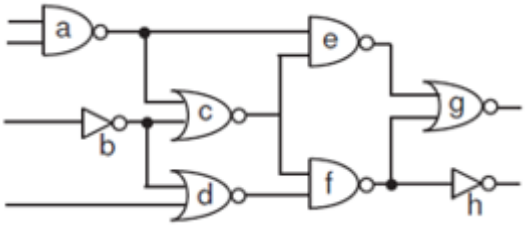

FIG. 3A

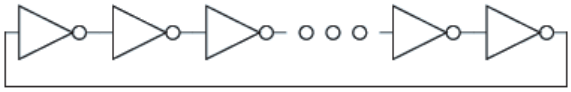

FIG. 3C

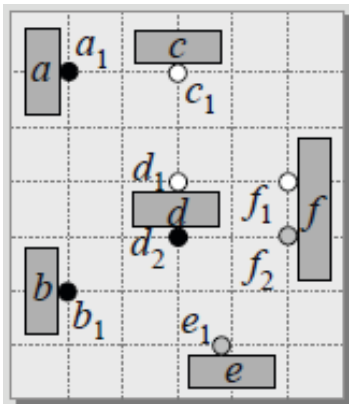

Fig. 4B

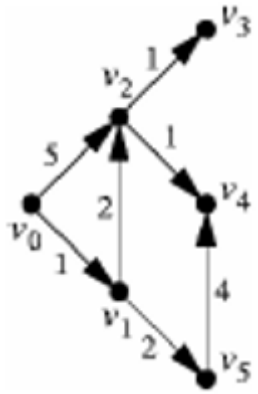

FIG 6A.

TABLE 5B		
	NS, z	
PS	X=0	X=1
A	B,0	E,0
B	E,0	D,0
C	D1	A,0
D	C,1	E,0
E	B,0	D,0