Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

SIXTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION
MAY/JUNE 2016
SUBJECT: ASIC DESIGN (ECE - 320)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Graph sheet will be provided.
- Missing data may be suitably assumed.

1A. Perform the Stockmeyer algorithm on slicing floorplan shown in **FIG.1A**. The (width, height) of the blocks 1 through 8 are *{*(2,4), (1,3), (3,3), (3,5), (3,2), (5,3), (1,2), (2,4)*}*. Assume that *xHy* means *x* is top and *y* is bottom, and *xV y* means *x* is left and *y* is right. Place the lower left corner of each block to the lower left corner of its room.

1B. Briefly explain the ASIC design flow with a neat diagram.

1C. Find the propagation delay and contamination delay for the circuit shown in **FIG. 1C**. a_0-a_6 are the arrival delays and the delay contributed by each gate is written inside the gate.

(5+3+2)

2A. Find the minimum number of tracks using left-edge algorithm. Given that

TOP	3	1	3	0	0	5	6	0	3	0	0	0
Bottom	1	2	4	2	4	1	5	7	0	7	6	0

2B. Braille is a system which allows a blind person to read alphanumeric by feeling a pattern of raised dots (●) given in **TABLE 2B**. Design a circuit that converts BCD to Braille and implement the same Xilinx FPGA

2C. What is fixed-die routing?

(5+3+2)

3A. Given the following locations of a clock source *s*0 (7,1) and eight sinks *s*1 (2,2), *s*2 (4,2), *s*3 (2,12), *s*4 (4,12), *s*5 (8,8), *s*6 (8,6), *s*7 (14,8) and *s*8 (14,6). (a) Draw the clock tree generated by MMM. (b) Draw the clock tree topology generated by MMM. (c) Calculate the total wire-length (in terms of grid units) and the clock skew using the linear delay model.

3B. Find the maximum operating frequency for the circuit shown in **FIG. 3B.**

3C. Explain working of SRAM Cell.

(5+3+2)

4A. Implement a code converter using PLA that converts BCD messages into Excess-3 code. The converter has four input lines carrying signals labeled *w*, *x* , *y*, and *z*, and four output lines carrying signals *f*1, *f*2, *f*3, and *f*4.

4B. What is Routing congestion? Given **FIG. 4B** placement *P* of blocks *a*-*f* and their pins (right), nets *N*1-*N*3, local vertical cut-lines *v*1-*v*6, local horizontal cut-lines *h*1-*h*6, and $\sigma P(e) = 3$ for all local cut-lines $e \in E$. find the wire density $\Phi(P)$ and determine the routability of *P* based on the RMST model. *N*1 = (*a*1, *b1*, *d2*) *N*2 = (*c*1, *d1*, *f1*) *N*3 = (*e*1, *f2*).

4C. Consider a process in which pMOS transistors have three times the effective resistance as nMOS transistors. Find the logical effort of three input NAND gate.

(5+3+2)

5A. Write a Verilog code for positive edge triggered D-flip flop using primitive and its test bench.

5B. For machine shown in **TABLE 5B**, find the equivalence partition and the corresponding reduced machine in standard form.

5C. Explain the partitioning. What is the quality of good partitioning?

(5+3+2)

6A. Draw the layout of 3-input CMOS NAND gate using shared contacted diffusion for reduced parasitic capacitance.

6B. Write a Verilog program to generate a clock signal for t_{on} and t_{off} 5 and 10 time unit respectively.

6C. What is week keeper circuit?

(5+3+2)

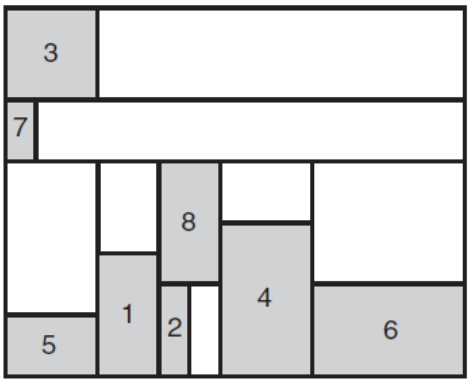

FIG. 1A

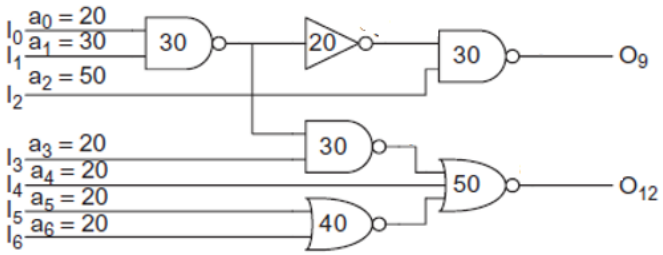

FIG. 1C

TABLE 2B

A	B	C	D	W	X	y
0	0	0	0		•	•
0	0	0	1			
0	0	1	0	•		
0	0	1	1	•	•	
0	1	0	0	•	•	•
0	1	0	1	•		•
0	1	1	0	•	•	
0	1	1	1	•	•	•
1	0	0	0	•		•
1	0	0	1		•	

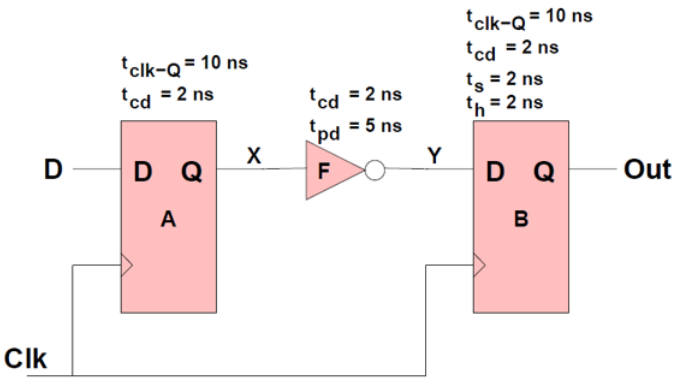

FIG. 3 B

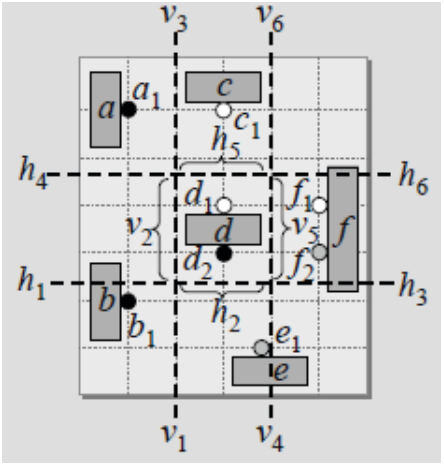

FIG. 4B

Table 5B		
	NS, z	
PS	X=0	X=1
A	E,0	C,0
B	C,0	A,0
C	B,0	G,0
D	G,0	A,0
E	F,1	B,0
F	E,0	D,0
G	D,0	G,0