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MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University



**SIXTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION
MAY/JUNE 2016**

SUBJECT: EMBEDDED SYSTEM DESIGN (ECE - 308)

TIME: 3 HOURS

MAX. MARKS: 50

Instructions to candidates

- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

- 1A. What is quality attribute in embedded system design? Explain the various operational quality attributes of embedded system.
- 1B. The 32bit data transfer instruction is 42918469h. Write the general instruction format and mention the significance of the given 32bit.
- 1C. Write the various data transfer types supported by USB and their use.

(5+3+2)

- 2A. Draw the functional block diagram of ARM processor. Explain the following in ARM processor: a) Register file b) Load store architecture c) Conditional execution d) ARM programming states.
- 2B. Explain the following i) Embedded firmware ii) Brown out protection circuit iii) Watch dog timer.
- 2C. The 8051 MC is interfaced to ADC and LCD through 8255. Draw the interface diagram showing all the control signals and data. Write the control word format for PPI for the given interface assuming PC used for control signals and PA and PB for data. Write an assembly code for initializing the MC.

(5+3+2)

- 3A. Draw an interface diagram to connect a switch (SW) and a stepper motor to P2.7 and P1.0-P1.3 of 8051 respectively. Write an embedded C program to do the following using suitable delay:
- i. If SW=0, the stepper motor moves clockwise
 - ii. If SW=1, the stepper motor moves anticlockwise
- Use full step sequence to rotate the stepper motor.

- 3B. Explain 'process' and 'thread' with the diagrams. Highlight the difference between process and thread.
- 3C. Write the valid difference between: i) Thumb and Thumb2 modes ii) AHB and ASB

(5+3+2)

- 4A. Explain the following wireless communication interface in brief: i) Ir DA ii) Bluetooth iii) Wi-Fi iv) Zigbee.
- 4B. Describe the 3-stage pipeline execution of the following sequence of ARM7 instructions till seven

clock cycles:

```
MOV r2, #8
BL    Square
ADD r1, r3, r3, LSL #1
SUBS r4, r4, r2
EORS r1, r3, r4
MOV r2, #5
STOP:  B STOP
Square:    MUL r3, r2, r2
ANDS r5, r3, r0
MOV PC, LR
End
```

- 4C. Three processes with process IDs P1, P2, P3 with estimated completion times 10, 5, 7 milliseconds and priorities 1, 3, 2 (0-highest priority, 3-lowest priority) respectively enter the ready queue together. A new process P4 with estimated completion time 4 ms with priority 0 enters the ready queue after 5 ms of start of execution of P1. Calculate the waiting time and turnaround time for each process and the average waiting time and turnaround time using pre-emptive shortest remaining time algorithm. Assume all the processes contain only CPU operation and no I/O time are involved.

(5+3+2)

- 5A. Draw the AMBA bus architecture and explain. Write the functional blocks used in the ARM cortex M3 processor with relevant advanced microcontroller bus types.
- 5B. Design an elevator controller unit based on FSM model for the following requirements:
- Move the elevator either up or down to reach the requested floor
 - Once at the requested floor, open the door for at least 10 seconds and keep it open until the requested floor changes
 - Ensure that the door is never open while moving.
 - Don't change directions unless there are no higher requests when moving up or no lower requests when moving down

Clearly mention the possible states, use following notations to indicate the actions that occur in each state: u, d, o, t.. An action that occurs is represented by '1', otherwise '0' and u->up, d->down, o->open, t->timer_start).

- 5C. Draw the CPSR format and mention the significance of each bit.

(5+3+2)

- 6A. What is task communication? Give the types. Explain the Remote procedure call in detail.
- 6B. Why are the following required in an embedded system? i) Memory controller ii) Interrupt controller iii) Initialization code
- 6C. Explain the following storage classes used in Embedded C program: i) far/xdata ii) sfr iii) sbit iv) code

(5+3+2)