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MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

**SIXTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION**
**MAY/JUNE 2016**
**SUBJECT: EMBEDDED SYSTEM DESIGN (ECE - 308)**

**TIME: 3 HOURS** **MAX. MARKS: 50**

**Instructions to candidates**
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. Explain the significance of the following: i) Memory shadowing ii)Brown-out protection circuit iii) Watch dog timer iv) Tightly coupled memory v) ONCE mode

1B. Write the format for MOV instruction and explain all the fields.

1C. The NRE cost and time to prototype involved in designing an ES is $500 and 1 month respectively. The unit cost involved in designing a single unit is $100 and the design turn-around time is 2months. Total 100 units are produced. Calculate the total cost and the time to market.

(5+3+2)

2A. Write the significance of a pipeline. Consider an ARM 3 stage pipeline, illustrate the pipeline operation with the help of a diagram for the sequence of code given below. Write the number of clock cycles required for the execution. What is the content of PC when "ADD" instruction is under execution? What is the content of r14 when "BL" instruction is under execution?

```
0x00000000  start: MOV r1,r2
0x00000004         CMP r1,r5
0x00000008         ADD r2,r5
0x0000000C         BL loop1
0x00000010         SUB r5,r7
0x00000014         END
0x00001000  loop1: ADDC r1, r3
0x00001004         MOV pc, r14.
```

2B. Describe the USB interface of LPC1768.

2C. Explain the following terms w.r.to an ES: i) Reactive and real time ii)Response and throughput

(5+3+2)

3A. Draw an interface diagram to connect 8 LEDs and two switches to P2 and P1.0 and P1.1 of 8051 respectively. Write an embedded C program to do the following using suitable delay:
   i. Turn ON and Turn OFF the LEDs when the SWITCH 1 is closed
   ii. Toggle EVEN and ODD LEDs alternatively when SWITCH 2 is closed

Otherwise generate the striking pattern ( i.e the pattern will be 0x81, 0x42, 0x24, 0x18, 0x18, 0x24, 0x42, 0x81)

3B. ARM instruction set differs from that of RISC. Justify the statement.

3C. Suggest a suitable communication interface used in embedded system:

i) Works on the principle of 'Shift Register'. The master and slave devices contain a special shift register for the data to transmit or receive.

ii)Supports multi-drop communication with one transmitter device and receiver devices up to 10

iii)Is intended for network communication and it supports Internet Protocol (IP) based communication

iv) Support a robust mesh network containing multiple nodes. This networking strategy makes the network reliable by permitting messages to travel through a number of different paths to get from one node to another.

(5+3+2)

4A. What is inter process communication (IPC)? Explain the following IPC: pipes, message queues, mailbox and socket.

4B. Write the valid difference between each of the following:
i) GPOS and RTOS. ii) Debugger and Emulator iii) 'C' and Embedded C

4C. List any four features of ARM cortexM3 processor which delivers high performance in microcontroller products.

(5+3+2)

5A. Write the various computational models used in the embedded system design and specify in which type of embedded systems they are used. Write the FSM model and sequential machine model to control the 3 floor lift. The given specifications are <S, r, u/d>; where $S_i$ is the floor i, $r_i$ is the request from floor i, $u_j/d_j$ is up/down to jth floor.

5B. What is a kernel? Write the types of kernel, their advantages and disadvantages. Mention the services provided by the Kernel.

5C. What is bit banding in ARM cortex processor? Analyse bit banding with the traditional method of bit access

(5+3+2)

6A. Draw the typical AMBA bus architecture and explain. Write the functional blocks used in the ARM cortex M3 processor with relevant advanced microcontroller bus types.

6B. Three processes with process IDs P1, P2, P3 with estimated completion time x, y, z milliseconds respectively enters the ready queue. The average TAT is 13ms and average waiting time is 5.66ms. The waiting time and execution time for process P3 is 5ms and 7ms respectively. The waiting time for process P2 is 0ms. TAT for P1 is 22ms. Assume there is no I/O waiting for the processes and all the processes contain only CPU operation and no I/O operations are involved. Complete the table shown below and also determine the scheduling algorithm adopted. Justify the answer.

| process | execution time | waiting time |
|---|---|---|
| P1 | x | a |
| P2 | y | b |
| P3 | z | c |

6C. List the different phases of EDLC.

(5+3+2)