Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

VI SEMESTER B.TECH (MECHATRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, JUNE/JULY 2016

SUBJECT: EMBEDDED SYSTEM DESING [ECE 356]

REVISED CREDIT SYSTEM

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ANY FIVE FULL q**uestions.
- Missing data may be suitably assumed.

1A. What is a kernel? Write a note on two types of kernels. **(4)**

1B. Illustrate the data path activity for STR (Store) instruction in ARM with a neat diagram. **(4)**

1C. Write a C program to toggle all bits of P2 continuously every 500ms. Use Timer 1, mode 2 to create the delay. **(2)**

2A. What are the quality attributes of Embedded system? Explain Non-operational quality attributes of Embedded system in detail. **(4)**

2B. Differentiate AMBA high performance bus (AHB), AMBA peripheral bus and AMBA system bus. Explain the two variations of AHB bus. **(3)**

2C. Design a coin operated public telephone unit based on FSM model for the following requirements. **(3)**

1. The calling process is initiated by lifting the receiver of the telephone unit.
2. After lifting the phone the user needs to insert a 1 rupee coin to make a call
3. If the unit is busy, the coin is returned on placing the receiver back on hook.
4. If the line is through, the user is allowed to talk until 60 seconds and at the end of 45 second, prompt for inserting another 1 rupee coin for continuing the call is initiated.
5. If the user doesnot insert another coin, call is terminated on completing 60sec time slot.
6. The system is ready to accept new call request when the receiver is placed back on hook.
7. The system goes to 'Out of order' state when there a line fault.

3A. Write a note on the following: **(4)**

i) Dynamic RAM
ii) Flash Memory
iii) Brownout protection circuit
iv) optocoupler

3B. Define pipelining? Describe the 5 stages of in 5-stage pipeline in ARM. **(3)**

3C. A switch is connected to pin PI.2. Write a C program to monitor SW and create the following frequencies on pin P1.7: **(3)**

SW=0: 500Hz
SW=1: 750Hz
Use Timer 0, mode 1 for both of them.

4A. Discuss ARM cortex M3. **(4)**

4B. List commonly used embed system design metrics. Illustrate time to market design metric and simplified revenue model for computing revenue loss from delayed entry. **(3)**

4C. Describe the advantages of Programmable Logic Devices. **(3)**

5A. Discuss the fundamental issues in hardware-software co-design. **(4)**

5B. Define non-preemptive multitasking? Three processes with process IDs P1, P2, P3 with estimated completion time 9, 6, 8 ms and priorities 1, 3, 4(0-highest priority, 3-lowest priority) respectively enters ready Q together. A new process P4 with estimated completion time 6ms and priority 0 enters the 'Ready' Q after 5ms execution of P1 and Process P5 with estimated completion time 5ms and priority 2 enters ready queue after 4ms of execution of P5. Calculate the waiting time and Turn Around Time (TAT) for each processes. Also Calculate the waiting time and TAT for each process and average waiting time and TAT (Assuming there is no I/O waiting for the processes) in priority based non-preemptive scheduling algorithm. **(4)**

5C. Explain pre indexed and post indexed addressing in ARM data transfer instruction. **(2)**

6A. Describe how exceptions are handled by ARM processor. **(4)**

6B. Explain the any two computational models in embedded system design. **(3)**

6C. Explain 'In System Programming'. What are the advantages of in system programming? **(3)**