Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIRST SEMESTER B.TECH DEGREE END SEMESTER EXAMINATION - NOV/DEC 2016

SUBJECT: BASIC ELECTRONICS (ECE - 1001)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Determine I_c, V_E, V_{CC}, V_{CE}, V_B and R_1 for the silicon transistor voltage divider bias circuit shown in the Figure Q1A. Given $I_B = 20$ µA.

1B. Explain the Zener breakdown mechanism. Draw the symbol and V-I characteristics of Zener diode.

1C. Draw V-I characteristics of silicon diode under forward biased condition. Also write diode current equation.

(5+3+2)

2A. Sketch the circuit of a bridge rectifier and describe its operation. Derive expressions for rectification efficiency and ripple factor without filter. If a capacitor filter is used, draw the output voltage waveform of the rectifier.

2B. Define line and load regulation with reference to voltage regulator. Draw the circuit diagram of a Zener regulator and obtain the expression for minimum and maximum value of input voltage for which the output voltage remains regulated.

2C. With the help of circuit diagram, explain the working of transistor as a switch.

(5+3+2)

3A. i) Write the expression for the output voltage at points X and Y for the circuit shown in Fig.Q3A given that $R_1 = R_2 = R = R_F = 10K\ \Omega$ and $C = 10\mu F$.

ii) Realize the equation $V_0 = 3V_1 - 0.5V_2 + 0.8V_3$ using OPAMP. Assume $R_F = 15K\Omega$.

3B. In a square wave generator using OPAMP, determine the value of the feedback resistor R connected to the inverting terminal for the following specification. Draw the circuit and voltage waveforms.

Frequency of oscillation = 10 KHz, Output Voltage: V_o (p-p) = 8V and Capacitor= 0.01µF and β = 0.5.

3C. For the OPAMP, define CMRR, Slew Rate, Input Offset voltage and Input Bias current.

(5+3+2)

4A. i) Subtract $(16.75)_{10}$ from $(26.25)_{10}$ using 1's compliment method.

ii) Simplify $F(A,B,C,D) = ABC + BCD' + A'BC$ using K-map and realize the function using NAND gates only.

4B. With a neat logic diagram and table explain the shifting of data 01101 (the right most bit is LSB which enters first) in Serial in and Serial Out mode for a 4 bit shift right register. Also mention how many clock cycles are required to shift the MSB of above mentioned data to the output.

4C. Obtain the expression for half subtractor and implement using basic gates.

(5+3+2)

5A. Derive the expression for AM wave (Assume sinusoidal modulation). Draw the frequency spectrum of AM wave and prove that the power in AM signal is $P_T = P_C\left(1 + \frac{m^2}{2}\right)$ where P_c is carrier power and m is modulation index.

5B. Draw the block diagram of digital communication system and explain the function of each block.

5C. Sketch the mesh and tree network topologies.

(5+3+2)

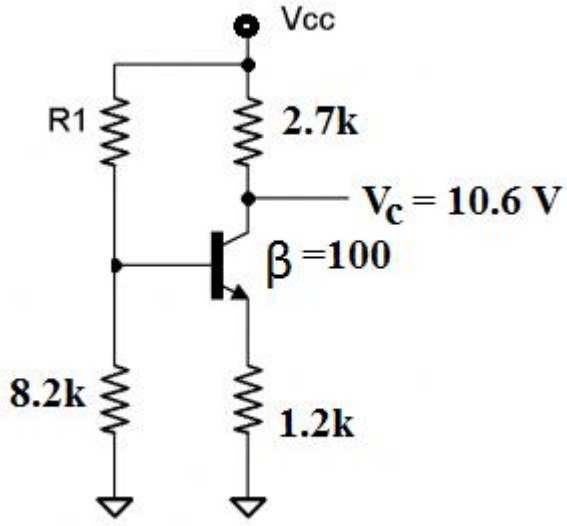

Fig. Q1A

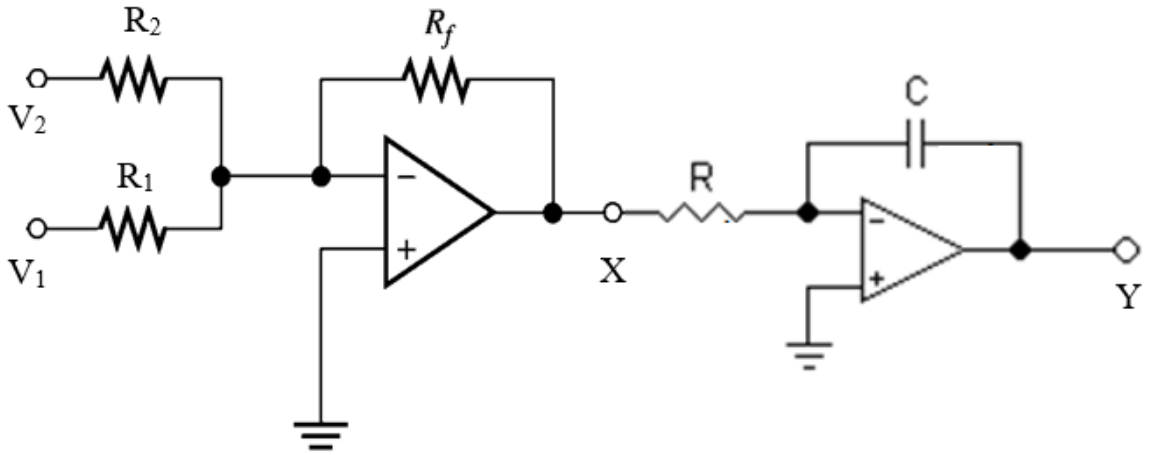

Fig. Q3A