Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIRST SEMESTER B.TECH DEGREE END SEMESTER EXAMINATION
NOV/DEC 2016
SUBJECT: BASIC ELECTRONICS (ECE - 1001)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. In the collector to base bias circuit given in Fig. Q1A, with $\beta = 100$ and $V_{BE}=0.7V$,
i) Determine the operating point.
ii) If β value increases by 50%, calculate the % change in collector current and collector to emitter voltage.

1B. Distinguish between Zener breakdown and Avalanche breakdown. Draw the V-I characteristics of Zener diode under reverse and forward bias conditions.

1C. Determine the diode current at 20°C for a silicon diode with reverse saturation current I_0= 50 nA and an applied forward bias of 0.6 V. If the temperature is increased to 100°C, what is the diode current?

(5+3+2)

2A. A half-wave rectifier has a load resistance of 3.5 kΩ. If the diode forward resistance is 10Ω and transformer secondary peak voltage is 15V, determine: (i) peak, rms and average values of current through load (ii) DC power output (iii) AC power input (iv) rectification efficiency.

2B. For the network shown in Fig. Q2B determine
i) V_{out}, I_L, I_Z, and I if R_L = 180 Ω
ii) The value of R_L that will establish maximum power conditions for the Zener diode
iii) The minimum value of R_L to ensure that the Zener diode is in the "on" state.

2C. Draw the circuit diagram of a typical R-C coupled amplifier. For sinusoidal input, sketch the input and output waveforms.

(5+3+2)

3A. With the relevant circuit diagram and waveforms, explain the working of OPAMP square wave generator. Write the expression for the frequency of the square wave output. Determine the resistance R required to obtain a square wave of frequency 10KHz. Given V_{CC} = 10 V, β = 0.5 and C= 0.01μF.

3B. For the circuit shown in Fig. Q3B, determine the output at each OPAMP and sketch V_0. Given V_1= 3V, V_2 = 10V, $R_f = R_1 = R_2 = R_g$ = 10KΩ. V_3=10 sin ωt and saturation voltage for each OPAMP is ±15V.

3C. Realize the equation $V_0 = 3V_1 + 5V_2 - 8V_3$ using OPAMP s. Assume R_F = 10kΩ.

(5+3+2)

4A. i) Subtract $(86.75)_{10}$ from $(63.25)_{10}$ using 2's complement.
ii) A combinational circuit with 4 inputs A, B, C, D that will produce output '1' for odd numbers from 0 to 9. Simplify using K map and Implement with NAND gates only.

iii) Simplify the expression using Boolean laws $f = (AB(C + (BD)') + (AB)')CD$

4B. Realize a 3-bit down counter using negative edge triggered JK flip flops. Draw the timing diagram for the same.

4C. Explain the working of NAND gate using discrete components.

(5+3+2)

5A. Define Frequency Modulation. Derive an expression for frequency modulated signal if the modulating signal is $A_m \cos(2\pi f_m t)$. Highlight the difference between FM and AM with reference to modulation index and bandwidth.

5B. Determine the power required (assuming R=1Ω) to transmit the signal shown in Fig. Q5B

5C. For the data shown in Fig.Q5C, sketch ASK and PSK signals.

(5+3+2)

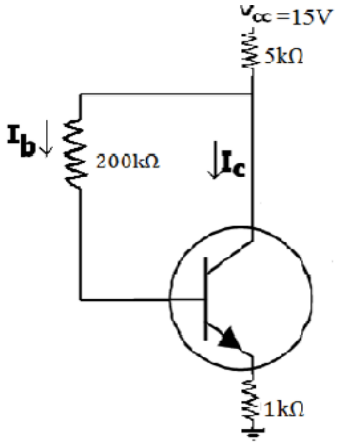

Fig Q1A

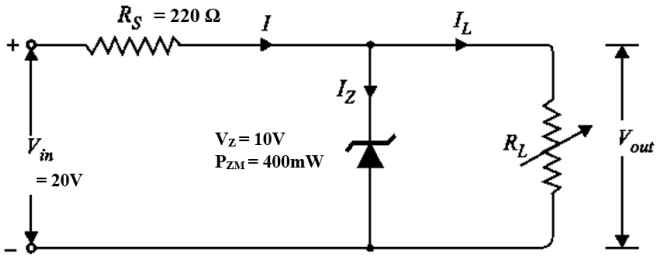

Fig. Q 2B

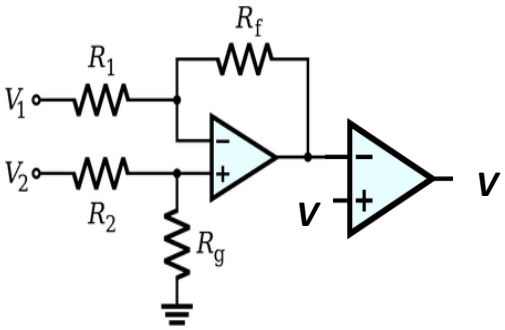

Fig. Q3B

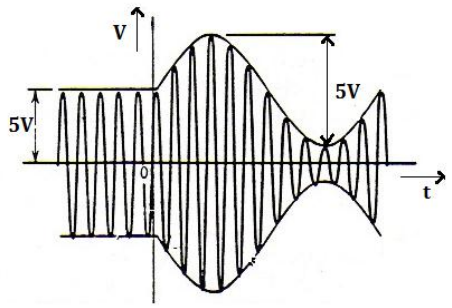

Fig. Q5B

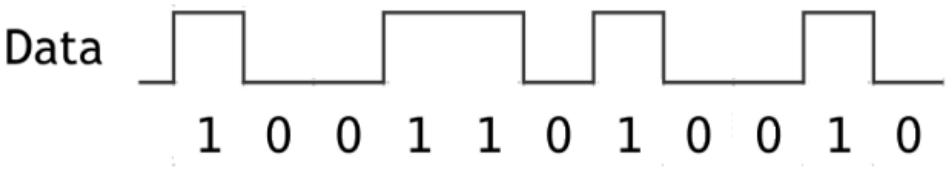

Fig. Q5C