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INTERNATIONAL CENTRE FOR APPLIED SCIENCES

(Manipal University)

III SEMESTER B.S. DEGREE EXAMINATION – NOV. / DEC. 2016

SUBJECT: COMBINATIONAL AND SEQUENTIAL LOGIC (EC 231)

(BRANCH: CS / CE / E&C / E&E & BM)

Friday, 2 December 2016

Time: 3 Hours **Max. Marks: 100**

- ✓ **Answer ANY FIVE full Questions.**
- ✓ **Missing data, if any, may be suitably assumed**

1A. (i) Add 548.6 + 280.37 in BCD number system.
(ii) Convert the following to the indicated bases $(34F.B)_{16} = (\ ?\ )_8$ $(84.3)_{10} = (\ ?\ )_2$
(iii) In an odd parity scheme which of the following contains an error?
(a) 10110111_2 (b) 11101010_2
(iv) Design a combinational circuit to detect the decimal numbers 0,2,4,6 and 8 in a BCD input.

1B. Simplify the following Boolean expressions.
(a) AB+(AC)'+AB'C(AB+C) (b) [A+(BC)']'(AB'+ABC)

1C. Write a dataflow VHDL code for 2 to 4 decoder. (10+5+5)

2A. Simplify the following function using karnaugh map and draw the circuit for the simplified expression using NAND gates. Also determine the essential prime implicant
F(A,B,C,D)=∑m(0,4,5,10,11,13,15)

2B. Design a combinational circuit to convert BCD to Excess 3 code using basic gates.

2C. Using Quine Mccluskey method, Obtain the minimal sum for
F(A,B,C,D)=∑m(2,3,4,6,9,11,12,13) (5+5+10)

3A. With a neat circuit diagram, explain the working of 4 bit binary adder/subtractor.

3B. Implement the following function F(A,B,C,D) = ∑m(0,1,3,4,8.9,15) using (i) 8:1 multiplexer and basic gates (ii) 4:1 multiplexer and basic gates.

3C. Implement the following multiple output combinational circuit using 4 to 16 decoder with active low outputs.
F1=∑m(0,1,2,6) F2=∑m(2,4,6) F3=∑m(0,1,5,6) F4=∑m(0,1,4,7,12,14,15)

3D. Write a behavioral VHDL code for 8:1 multiplexer using case statement (5+5+5+5)

4A. Implement the following function using PLA F=∑m(0,2,4,6,7,8,10,12,13,15)

4B. Design a circuit for 4 to 2 priority encoder using basic gates.

4C. Convert (i) JK flipflop to SR flipflop, (ii) SR flipflop to T flipflop.

4D. Design a Mod 6 ripple up counter using T flipflop (5+5+5+5)

5A. Design a synchronous counter that goes through states 0,1,2,4,0,….The unused states must always go to zero (000) on the next clock pulse.

5B. Explain the operation of a master slave JK flipflop with a neat circuit diagram.

5C. Draw the logic diagram of gated SR latch using NAND gates. Derive the truth table for the same and explain its operation. (10+5+5)

6A. With a neat circuit diagram, explain the operation of 4 bit Universal Shift register.

S_1	S_0	Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

6B. Reduce the following state table and draw reduced state diagram.

Present State	Next State		Output	
	X=0	X=1	X=0	X=1
A	B	C	1	0
B	F	D	0	0
C	D	E	1	1
D	F	E	0	1
E	A	D	0	0
F	B	C	1	0

6C. Write the behavioral VHDL code for 4 bit parallel in serial out shift register (10+5+5)

7A. Analyze the following synchronous sequential circuit. Draw the logic circuit, excitation table / state table and state diagram. (X is the input, A&B are the outputs)

$J_A=B$, $J_B=X'$, $K_A=X'B$, $K_B=A$ xor X

7B. Design a Mealy type Sequence detector to detect an overlapping sequence “110” (10+10)

8A. Write the structural VHDL code for 4 bit binary parallel adder using full adders (Code needs to be written for entire hierarchy)

8B. Explain the operation of Johnson counter with a neat circuit diagram and suitable timing waveforms.

8C. Define the following terms with an example

(i) Self complementing code

(ii) Unit distance code

(10+5+5)