Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

III SEMESTER B.Tech (BME) DEGREE MAKE UP EXAMINATIONS DEC/JAN 2016-17
SUBJECT: ANALOG ELECTRONICS (BME 2102)
(REVISED CREDIT SYSTEM)
Monday, 26th December 2016, 9 AM to 12 NOON

TIME: 3 HOURS **MAX. MARKS: 100**

Instructions to Candidates:

1. **Answer ALL questions.**
2. **Draw labeled diagram wherever necessary**

1. **(a)** i) A typical fixed bias circuit has $R_B = 470k\Omega$, $R_C = 2.2k\Omega$ and $V_{CC} = 18V$ with a transistor having $h_{FE} = 100$. Determine the base current, collector current and collector to emitter voltage. **4+4**

ii) The figure Fig 1A below shows that a silicon transistor with β = 100 is biased by base resistor method. Draw the dc load line and determine the operating point.

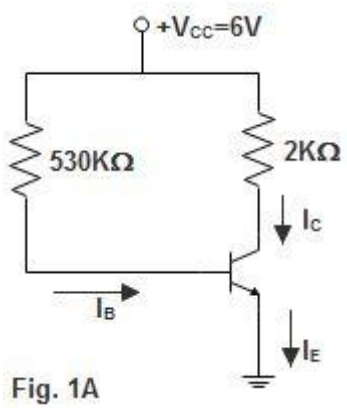

Fig. 1A

(b) Derive an expression for the factor that describes the stabilization of collector current against variations in the value of base emitter voltage, keeping the values of reverse collector saturation current and β constant. **6**

(c) Draw the approximate small signal model for the common collector transistor amplifier configuration, and find the expressions for: voltage gain, current gain, input resistance and output resistance. **6**

2. **(a)** A three stage RC coupled amplifier used BJT's with the following parameters: $h_{fe} = 50, h_{ie} = 1.1K$, $h_{re} = h_{oe} = 0$. $R_c = 2K, R_1 = 20K$, $R_2 = 20K$, $R_e = 1K$, $C_b = 0.005\mu F$ and C_e represents a short for each stage. **8**

a) Evaluate overall mid band voltage gain in dBs.

b) Low 3-dB frequency

c) High 3-dB frequency

d) Overall low and high 3-dB frequencies.

(b) Express common collector $h-$parameters in terms of common emitter $h-$parameters. **6**

(c) What is a direct coupled transistor amplifier? With a circuit diagram analyze its biasing aspects. How different it is from RC coupled amplifier? **6**

3. **(a)** i) An amplifier has an open-loop gain Av = 100,000. A negative feedback of 10 dB is applied. Find (i) voltage gain with feedback (ii) value of feedback factor β. **4+4**

ii) An amplifier has a voltage gain of 1000 without feedback. If a negative feedback is applied, the gain is reduced to 100. Calculate the fraction of the output fed back. If, due to ageing of components, the gain without feedback falls by 30%, calculate the percentage fall in gain with feedback.

(b) What do you understand by negative feedback? How does negative feedback affect the input impedance and output impedance of an amplifier? Justify by considering voltage series feedback amplifier. **6**

(c) Design a current series feedback amplifier circuit with the following specifications: Input resistance with feedback is 50 KΩ. **6**

4. **(a)** i) The ac equivalent circuit of a crystal have these values: L = 1H, C = 0.01 pF, R = 1000 Ω and C' = 20 pF. Calculate f_S & f_P of the crystal. **8**

ii) Prove that the ratio of parallel to series resonant frequency is given by $\left(1+\frac{1}{2}\frac{C}{C^1}\right)$

(b) How does an FET RC phase shift oscillator circuit work? Derive an expression for its frequency of oscillations. **6**

(c) Design a colpitts oscillator circuit that generates oscillations having a frequency of 250 KHz. The stability factor is 6. **6**

5. **(a)** i) For a class B amplifier providing a 20-V peak signal to a 16-Ω load (speaker) and a power supply of V_{CC} = 30 V, determine the input power, output power, and circuit efficiency. **4+4**

ii) For the circuit shown below in Fig 5, find the quiescent values of drain current, gate source voltage and drain source voltage of the FET. The pinch off voltage is $-8\,V$ and drain source saturation current is 10 mA.

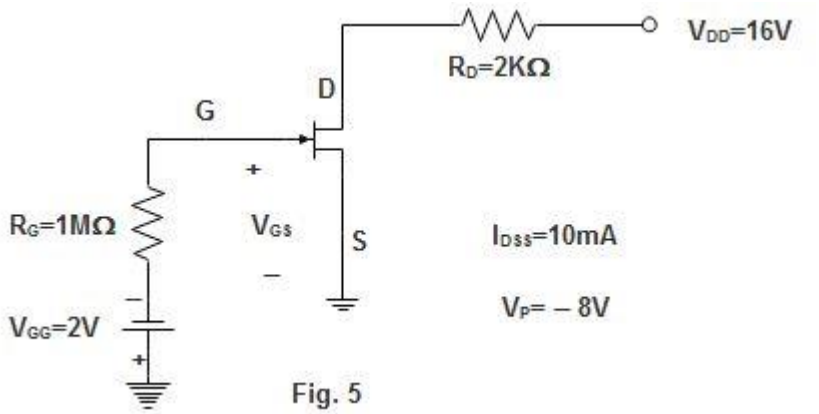

Fig. 5

(b) How does a series fed class A power amplifier work? Derive its efficiency in terms of dc power and ac power. **6**

(c) Draw the n - channel enhancement type MOSFET using the collector to base bias concept. Determine the quiescent values of gate source voltage and drain current. The following parameter values are provided: **2+4**

$V_{DD} = 12V, I_D = 6mA, V_{DS} = 8V, V_{GS(Th)} = 3V, R_D = 2K\Omega.$