Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

III SEMESTER B.TECH. (COMPUTER AND COMMUNICATION ENGG.)

MAKE UP EXAMINATIONS, DECEMBER 2016

SUBJECT: DIGITAL SYSTEM DESIGN [ICT 2151]

REVISED CREDIT SYSTEM
(28/12/2016)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Design a code converter to convert a decimal digit represented in 8 4 -2 -1 to decimal digit represented in excess -3 code, using NAND gates only. **(05)**

1B. Using 74153 IC and external NAND gates, design a full adder. **(03)**

1C. Design MOD–8 ring counter using JK – flip flops. Also write all the states of the counter. **(02)**

2A. Design a synchronous 3- bit gray code UP/DOWN counter using JK – flip flops and external gates. **(05)**

2B. Derive the characteristic equation of SR flipflop. **(03)**

2C. Design a 4- bit magnitude comparator using 7483 IC and NOR gates only. **(02)**

3A. Design a sequence detector with one input Y and one output Z. The output Z is HIGH whenever the sequence "00010" is detected, otherwise the output is LOW. Overlapping of the sequence is allowed. Implement using D - flip flops and minimum external gates. **(05)**

3B. Divide $(1110)_2$ by $(0100)_2$ using non restoring division algorithm. Indicate all the steps. **(03)**

3C. Show that, each state of a MOD-6 Johnson counter can be decoded using a two input AND gate. **(02)**

4A. Design a hardwired control unit for 4x4 Booth's multiplier. **(05)**

4B. What is Race around condition in JK – Flip Flop? With necessary diagram, explain how master–slave JK – flip flop overcomes the same. **(03)**

4C. Design a 4-to- 2 priority encoder using NOR gates only. **(02)**

5A. Design the combinational circuit to evaluate the algebraic expression, F=(X+Y) (X-Y) using full adders and external NAND gates, where X and Y are two bit binary numbers. **(05)**

5B. Design SR – flip flop using NOR Latch. **(03)**

5C. Differentiate between direct and associative cache mapping techniques. **(02)**