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# MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL

A Constituent Institution of Manipal University

## III SEMESTER B.TECH.(COMPUTER AND COMMUNICATION ENGINEERING)

### END SEMESTER EXAMINATIONS, NOV/DEC 2016

## SUBJECT: DIGITAL SYSTEM DESIGN [ICT 2151]

### REVISED CREDIT SYSTEM
### ( 25 /11/2016)

Time: 3 Hours MAX. MARKS: 50

**Instructions to Candidates:**

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

**1A.** Design a 4-bit binary Carry Look Ahead adder circuit. Discuss its merits over conventional 4-bit binary ripple carry adder. **(05)**

**1B.** Design asynchronous counter using negative edge triggered JK – flip flops to generate a square waveform (50 % duty cycle) of frequency $\frac{1}{12}$ of input clock waveform. Also draw the waveforms. **(03)**

**1C.** Design a JK – flip flop using D – flip flop and external gates. **(02)**

**2A.** Design a synchronous UP/DOWN counter using JK – flip flops and external gates to count the sequence $1 \rightarrow 3 \rightarrow 6 \rightarrow 7 \rightarrow 2 \rightarrow 1$. **(05)**

**2B.** Design a logic circuit to evaluate the arithmetic expression $(A^2 - B^2)$ using 7483 IC and external gates. A and B are 3-bit binary numbers with A > B. **(03)**

**2C.** Using 7490 IC and minimum external gates, design a sequential circuit to generate the sequence 00111011. **(02)**

**3A.** Design microprogrammed control unit for 4 x 4 Booth's multiplier. **(05)**

**3B.** Divide $(1101)_2$ by $(0101)_2$ using restoring division algorithm. Indicate all the steps. **(03)**

**3C.** Design a MOD – 10 twisted ring counter using JK – flip flops. Also write all the states of the counter. **(02)**

**4A.** Design a code converter to convert a decimal digit represented in gray code to decimal digit represented in 8 4 -2 -1 code, using 74138 ICs and external gates. **(05)**

**4B.** Using 74193 ICs and external gates, design a 2 – digit hexadecimal down counter which counts from 87H to 19H and repeats. **(03)**

**4C.** Explain salient features of a set associative mapped cache memory. **(02)**

**5A.** Design a sequence detector with one input Y and one output Z. The output Z is HIGH whenever the sequence "110111" is detected, otherwise the output is LOW. Overlapping of the sequence is allowed. Implement using T- flip flops and minimum external gates. **(05)**

**5B.** Design 2-bit magnitude comparator with cascading inputs. Using the same, design a 4-bit magnitude comparator. **(03)**

**5C.** What is "Self complementing code"? Explain a non-weighted self-complementing code. **(02)**