Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

III SEMESTER B.TECH. (COMPUTER SCIENCE AND ENGINEERING)

END SEMESTER EXAMINATIONS, NOV/DEC 2016

SUBJECT: COMPUTER ORGANIZATION AND DESIGN [CSE 2101]

REVISED CREDIT SYSTEM
(23/11/2016)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitable assumed.

1A. Prepare a table showing any five main characteristics of RISC and CISC based machines. Write a program which adds a list of numbers using CISC-style instructions. **4M**

1B. Explain the three truncation methods for the guard bits of floating point numbers with truncated mantissa of 3 bits, considering 3 guard bits. Explain the different levels of implementing parallelism to increase the performance? **4M**

1C. Perform the multiplication of 1011 with 1111 using carry-save addition. For this example, give the schematic representation of CSA tree. **2M**

2A. Starting from basic principles obtain the expressions for *Generate* and *Propagate* functions of 4-bit CLC. From the derived expression obtain a bit-stage cell. Using these cells and 4-bit CLC, construct a 4-bit CLA. **4M**

2B. Perform a fast multiplication of the multiplicand 13 by the multiplier -6 using bit-pair recoding of the multiplier method. Write the related table of multiplicand selection decisions. **3M**

2C. Design a 4 bit ALU that will meet the following specification. **3M**

S1	S0	operation
0	0	A plus B
0	1	B
1	0	A OR B
1	1	A′

3A. Consider the Register transfer description given below. Registers A, M, Q are 4-bits in size, L is a 3 bit register, C is a 1-bit register and C_{out} is the carry generated from Adder.

Declare registers A[4], M[4], Q[4], L[3], C[1];
Declare Inbus[4], Outbus[4];

START: A←0, M←Inbus, L←4, C←0;
Q←Inbus;
LOOP: if Q[0]= 1 then goto ADD;
Goto SHIFT;
ADD: A←A+M;
C← C_{out};
SHIFT: LSR(C $ A $ Q);
L←L-1;
if L< > 0 then Go to LOOP;
Outbus = A;
Outbus = Q;
HALT: Go to HALT;

Write the symbolic microprogram and design micro programmed control unit for this microprogram assuming that number of control signals sent from your control unit to the processing section is 12. **4M**

3B. Write the Programmable Logic Array (PLA) truth table and its implementation using AND and OR arrays for the following equation, where X, Y, Z, T1, T2, and T3 are the inputs and the rest are outputs of PLA.

P0= X Y′ Z T1 P1=X Y Z T2 P2=X′ Y Z′ T2 P3=X′ Y′ T3

K=P0+P1+P2+P3 m3=P0+P2 m2=P0+P1+P2 m1=P2+P3

m0=P1+P2+P3 **4M**

3C. Build hardware to implement the following register transfer.
If X is even then A←B *OR* C
Else A←B *AND* C
Assume A, B, C and X are 4 bit registers. **2M**

4A. Draw the internal organization of a 19 X 16 memory chip showing at least two rows of cells constituting a memory word. Explain its operation. **4M**

4B. A set-associative cache consists of a total of 64 blocks divided into 4-block per set. The main memory contains 4096 blocks, each consisting of 128 words.
(a) Draw the diagram to meet the above mapping technique.
(b) How many bits are there in a main memory address?
(c) How many bits are there in each of the TAG, SET, and WORD fields? **4M**

4C. Define the following:
(i) Memory Cycle Time (ii) Latency Time (iii) Data Striping (iv) Miss Penalty **2M**

5A. Explain in detail how the Write buffer supports in enhancing the performance of a computer when write-through and write-back protocols are used. **4M**

5B. With appropriate diagram illustrate the concept of interrupts assuming that an interrupt request arrives during execution of instruction *i*. **3M**

5C. What is DMA. Explain the importance of DMA controller with the help of diagram. **3M**