Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

III SEMESTER B.TECH. (COMPUTER SCIENCE AND ENGINEERING)

MAKEUP EXAMINATIONS, DEC 2016 - JAN 2017

SUBJECT: SWITCHING CIRCUITS AND LOGIC DESIGN [CSE 2102]

REVISED CREDIT SYSTEM
(28/12/2016)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitable assumed.

1A. Simplify the following expression using Boolean algebra **2M**
F (A, B, C) = $\overline{A}\overline{B}\overline{C}$ + $\overline{A}\overline{B}$C + $\overline{A}$B$\overline{C}$ + A$\overline{B}\overline{C}$ + A$\overline{B}$C

1B. A circuit with two outputs has to implement the following functions **4M**

f (x1, . . . , x4) = $\sum$m(0, 2, 4, 6, 7, 9) + D(10, 11)
g(x1, . . . , x4) = $\sum$m(2, 4, 9, 10, 12, 15) + D(0, 13, 14)

Design the minimum-cost SOP implementation and compare its cost with combined costs of two SOP implementation that implement f and g separately. Assume that the input variables are available in both uncomplemented and complemented forms.

1C. Consider the function **4M**

f = x3x5 + x1'x2x4 + x1x2'x4' + x1x3x4' + x1'x3x4 + x1'x2x5 + x1x2'x5.

Use factorization to derive minimum cost circuit that implements this function using only NAND gates and draw the circuit diagram.

2A. Write Verilog code for three bit multiplier using half adder and full adder modules. **3M**

2B. Design a 4 bit comparator circuit using 4 bit subtractor circuit. Derive the expressions for A=B, A<B and A>B, where A and B are 2 four bit numbers. **5M**

2C. With example show the two cases where correction has to be made during the addition of two BCD digits. Also show the result after correction. Using four bit binary adders, design the single digit BCD adder by deriving expression for the above correction. **2M**

3A. For the function F(A, B, C, D) = ∑m(1, 2, 3, 7, 8, 9, 10, 12), use Shannon's expansion with respect to AB, to derive an implementation using 4:1 multiplexer and minimum number of additional gates. **3M**

3B. A combinational circuit building block receives an 8 bit input A_{7-0}, and produces a 3 bit output Y_{2-0} and one 1 bit output Z. Y indicates the most significant bit of the input that is TRUE. Z should be TRUE if there are one or more TRUE bits on the input. What is this building block? Draw the block diagram and the truth table. **3M**

3C. Design a 3 to 8 decoder using 2 to 4 decoders. Write the hierarchical Verilog code for 3 to 8 decoder using these 2 to 4 decoders. Use for loop to design 2 to 4 decoders. **4M**

4A. Design a synchronous counter with the following repeated binary sequence: 3, 4, 7, 2, 6, 9, 15, 11, 13, 8.Use T flip-flop. Direct the unused 0 state to 3. Treat the other unused states as don't care conditions. **5M**

4B. Draw the logic diagram of a 4 bit register with four D flip flops and four 4:1 multiplexers with mode selection inputs s1 and s0. The register operates according to the following function table given below. **2M**

S1	S0	Register operation
0	0	No change
0	1	Complement the 4 outputs
1	0	Clear register to 0
1	1	Load parallel data

4C. Construct a JK Flip Flop using AND and NOR gates. Write the characteristic table of this Flip Flop considering all possible combinations of input and present state. What is the undesirable operation of the above construct? Mention the solutions used to overcome it. **3M**

5A. Explain the following with neat diagrams. **2M+2M**

a) PMOS transistor as a switch
b) NMOS realization using NAND gates.

5B. Define tristate buffer. Explain four types of tristate Buffers with neat diagrams. **3M**

5C. The logic diagram of a sequential circuit is given in Figure Q5.C. Derive the state table and state diagram of the circuit. **3M**

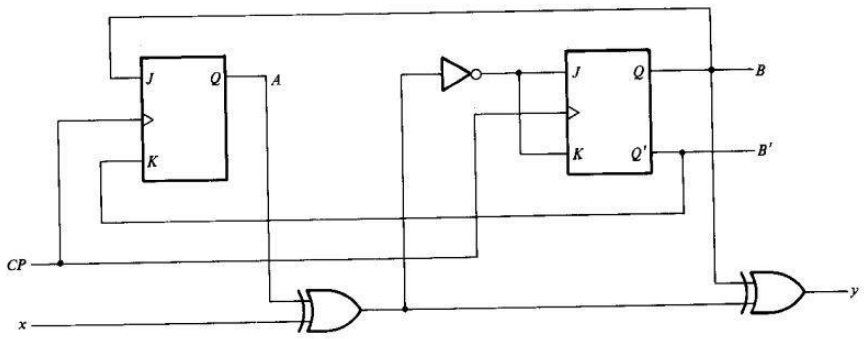

Figure Q5.C

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