Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

III SEMESTER B.TECH. (COMPUTER SCIENCE AND ENGINEERING)

END SEMESTER EXAMINATIONS, NOV/DEC 2016

SUBJECT: SWITCHING CIRCUITS AND LOGIC DESIGN [CSE 2102]

REVISED CREDIT SYSTEM
(25/11/2016)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitable assumed.

1A. Use K-map to obtain the simplest SOP and POS expressions for the function f(a,b,c,d)=πM(2,6,7,10,11,13,14,15). Design the minimum cost NAND circuit for this function. What is the minimum cost? Assume that input variables are available in uncomplemented form only. **4M**

1B. Derive the simplest SOP expression for the following function using Boolean Algebra.

$$f(a,b,c,d,e) = a'c'e' + a'c'd' + a'de + ab'c'e$$

4M

1C. For the timing diagram in Figure Q1C., write the truth table and synthesize the function f (x_1, x_2, x_3) in the simplest SOP form using K-map. Also write the essential prime implicants.

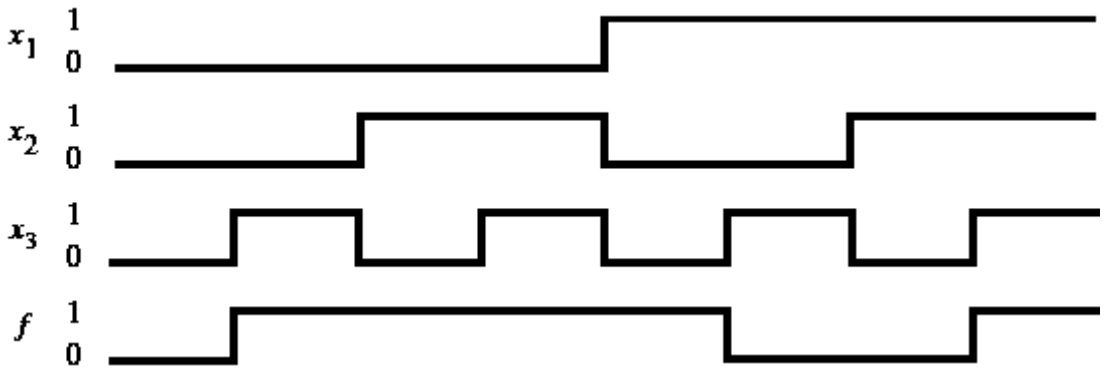

Figure Q1C. **2M**

2A. i) Design a four bit adder/subtractor and explain its operation. What do you mean by arithmetic overflow? Write the expression which indicates arithmetic overflow for n-bit addition.

ii) If A = $A_7A_6A_5A_4A_3A_2A_1A_0$ is an 8-bit unsigned number then 2A = $A_7A_6A_5A_4A_3A_2A_1A_0$0. Use this concept to design a circuit that multiplies an 8-bit unsigned number by 3, using single 9-bit ripple carry adder. Explain its operation. **(3+2)M**

2B. Design a combinational circuit that adds one to a 4-bit binary number, $A_3A_2A_1A_0$ using half adders. Write the Verilog code for your design using vectors. Use half adder module in your code. **3M**

2C. Design a counter with T Flip Flops that repeats the binary sequence 0, 1, 3, 5, 7. Treat unused states as don't care conditions. **2M**

3A. Apply shannon's expansion to the following function with respect to *a, d* and implement using only 4 to 1 multiplexers.

$$f(a,b,c,d,e) = a'b'd'e' + ab + ac + ad + cde$$

Write the Verilog code for 4 to 1 multiplexer using conditional operator and using this module write the Verilog code for your design. **4M**

3B. Write the truth table for BCD to 2421 code converter. Design this code converter using 2 to 1 multiplexers and other necessary gates **4M**

3C. A combinational circuit is specified by the following three Boolean functions. Implement the circuit with 3 to 8 decoder and other necessary gates. Minimize the number of inputs to the gates.
F1(A,B,C) = ∑m(2,4,7)
F2(A,B,C) = ∑m(0,3)
F3(A,B,C) = ∑m(0,2,3,4,7)
Write Verilog code for your design. Use case statement. **2M**

4A. Design a sequential circuit with two JK Flip Flops, A and B, and two inputs E and x. If E=0, the circuit remains in the same state regardless of the value of x. When E=1 and x=1, the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00 and repeats. When E=1 and x=0, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00 and repeats. **5M**

4B. With the help of a neat diagram, explain the working of positive edge triggered D Flip Flop for all cases of D and clock inputs. What do you mean by set up time and hold time? **3M**

4C. Draw the circuit for a 4-bit Ring counter using a counter and a decoder. Write the count sequences and draw the timing signals generated. **2M**

5A. What is a tri state buffer? Explain its types and one application. **5M**

5B. Explain CMOS realization of NAND and AND gates with necessary circuit diagrams. **3M**

5C. Implement the following functions using PLA. Use minimum no. of AND gates and OR gates with minimum inputs.
F1(A,B,C)=∑m(3,4,6,7)
F2(A,B,C)=∑m(0,1,3,4) **2M**