Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

III SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

MAKEUP EXAMINATIONS, DEC 2016 - JAN 2017

SUBJECT: DIGITAL ELECTRONIC CIRCUITS [ELE 2102]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 30 December 2016** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Design a logic circuit to implement f (a,b,c,d) = $\sum m(5,7,8,14) + d(0,1,2,3,10,12,13)$ using minimum number of NAND gates only ***(03)***

1B. Simplify the following using VEM technique with E as MEV.

$$f(A,B,C,D,E) = \sum m(1,2,4,5,6,7,12,13,15,18,20,21,22) + d(23,24,25,26,27,28,29,30,31)$$

(05)

1C. Using 74LS194 wired as a left shift register implement ring counter. ***(02)***

2A. Design a gray to BCD converter using 3 to 8 decoders. Residual gates may be used. ***(04)***

2B. Develop 16 to 1 multiplexer using 4 to 1 multiplexers.. ***(04)***

2C. Design a 3 bit even parity checker circuit. ***(02)***

3A. Design a synchronous 3 bit binary up/down counter using JK Flip flops. ***(06)***

3B. Using 74LS283 implement single byte adder/subtract or. ***(02)***

3C. Design a mod 6 counter using IC 7490 ***(02)***

4A. Simplify f(A,B,C,D) = $\sum m(1,4,5,9,11,12,14) + d(3,13,15)$ using Quine McCluskey (QM) method. ***(04)***

4B. Draw and explain a CMOS circuit to implement 2 input AND circuit. ***(03)***

4C. Which are the asynchronous inputs of Flip Flops? State their importance. ***(03)***

5A. Convert JK Flip flop to T Flip flop ***(03)***

5B. Design a Mealy machine to detect the sequence 0110 and 1001 using D Flip flops. Implement Next State Decoder and output Decoder using 4 to 1 multiplexers ***(07)***