Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

III SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

END SEMESTER EXAMINATIONS NOV/DEC 2016

SUBJECT: DIGITAL ELECTRONIC CIRCUITS [ELE 2102]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 28 November 2016** **MAX. MARKS: 50**

Instructions to Candidates:

- Answer **ALL** questions.
- Missing data may be suitable assumed.

1A. Design a logic circuit to implement f (a,b,c,d) = $\sum m(1,3,5,9,11,12,13,14) + d(2,6,8)$ using minimum number of NOR gates only ***(03)***

1B. Simplify f(A,B,C,D,E) = $\sum m(0,5,8,9,10,21,26,29,30) + d(1,7,12,13,14,15,16,17,20,22,25,27)$ using VEM technique ***(05)***

1C. Using 74LS194 wired as a right shift register implement Johnson counter. ***(02)***

2A. Design a 4 bit binary to gray code converter using 3 to 8 decoders. Residual gates may be used. ***(04)***

2B. Realize the Boolean expression

f(w,x,y,z) = ∑m(0,2,4,5,7,9,10,14)

Using a multiplexer tree structure. The first level should consist of two 4-to-1 line multiplexers with variables w and z on their select lines S1 and S0 , respectively, and second level should consist of a single 2-t0-1 line multiplexer with the variable y on its select line. ***(04)***

2C. State the importance of valid bit in 4 to 2 Priority encoder, with the help of relevant truth table ***(02)***

3A. Draw the state diagram of a synchronous 3 bit counter which works as a mod-8 binary counter when an input control signal G=0 and as a mod-8 gray code counter when G=1. Design and implement the counter using T flip flops. ***(05)***

3B. Using 74LS283 implement one digit BCD adder. ***(03)***

3C. Design a Divide by 10 counter using IC 7493 ***(02)***

4A. Simplify f(A,B,C,D,E) = $\sum m(1,8,21,28) + d(4,5,12,17,24,25,26,27,30)$ using Quine McCluskey (QM) method. ***(04)***

4B. Mention the different blocks with their significance in the Algorithmic State machine Chart. Draw the ASM chart for a 4 to 1 multiplexer. ***(04)***

4C. Draw the output waveforms (Q1, Q2) of the circuit given in Figure Q4C. ***(02)***

5A. AB flip flop has a characteristic equation $Q^+ = BQ + A\overline{Q}$. Construct AB flip flop using T Flip flop ***(04)***

5B. In a 10 bit input stream, count the no of occurrence of the sequence 010 as a Mealy machine. Implement using D flip flop and IC 74LS90. ***(06)***

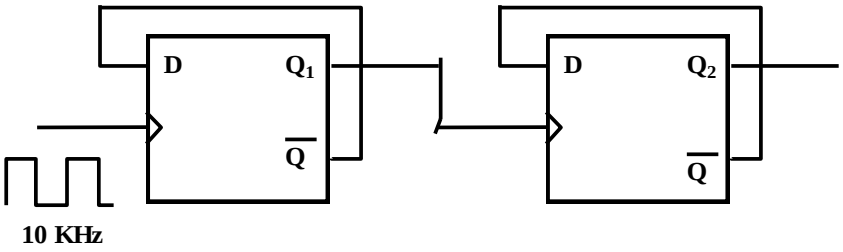

Figure Q 4C