Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

THIRD SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2016
SUBJECT: ANALOG ELECTRONIC CIRCUITS (ECE - 2101)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates:
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Design a single stage amplifier which gives a voltage gain of 5 without any change in the phase of the signal and an input impedance of 100Ω. Assume β=100, V_{CC}=2.5V, Is=10^{-16}A, V_A=∞ and operating frequency of 700MHz.

1B. In the circuit of Fig. Q1 (B), β=100 and V_A=∞. Calculate the value of I_S such that the base-collector junction is forward biased by 200mV.

1C. A voltage dependent current source is constructed with K=20mA/V. What value of load resistance in Fig. Q1 (C) is necessary to achieve a voltage gain of 15?

(5+3+2)

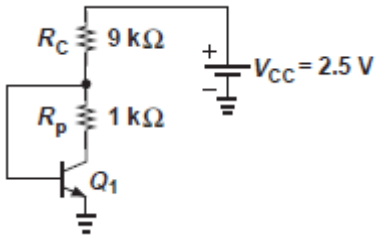


Fig. Q1 (B)

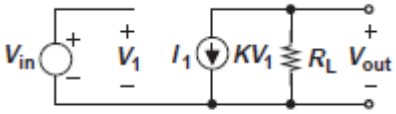


Fig. Q1 (C)

2A. The circuit of Fig. Q2 (A) must be designed for an input impedance of greater than 10kΩ and a g_m of at least 1/(260Ω). If β=100, I_S=2×10^{-17}A, and V_A=∞, determine the minimum allowable values of R_1 and R_2. If the design is to be repeated for a g_m of at least 1/(26Ω), show that no solution exists.

2B. In Fig. Q2 (B), calculate the bias current of M_1. Assume $\mu_n C_{ox}$ = 100μA/V^2 and V_{TH} = 0.4V. Verify if the device is operating in saturation. If the gate voltage increases by 10mV, what is the change in the drain voltage? Determine the value of W/L that places M_1 at the edge of saturation. Calculate the drain voltage change for a 1mV change at the gate.

2C. In the I_D–V_G plot of Fig. Q2 (C), the arrow indicates (i) Decreasing channel length 'L' (ii) Decreasing oxide thicknesses 't_{ox}' (iii) Increasing channel width 'W'. Identify the correct statements. Correct the statements which are incorrect.

(5+3+2)

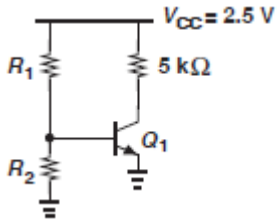


Fig. Q2 (A)

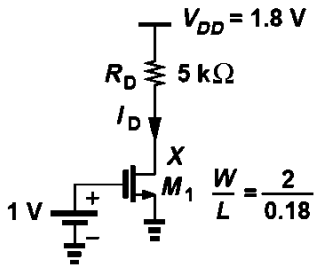


Fig. Q2 (B)

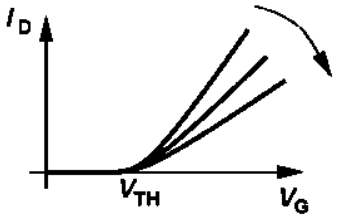


Fig. Q2 (C)

3A. For the amplifier circuit shown in Fig. Q3 (A), neglecting channel length modulation, derive the expression for the voltage gain. Assuming a power budget of 1mW and an overdrive voltage of 200mV for M_1, design the circuit for a voltage gain of 4.

3B. Using Miller's theorem, determine the input capacitance of the circuit shown in Fig. Q3 (B). Assume $\lambda>0$.

3C. Construct the MOSFET circuit using the small signal model shown in Fig. Q3 (C). Is your solution unique?

(5+3+2)

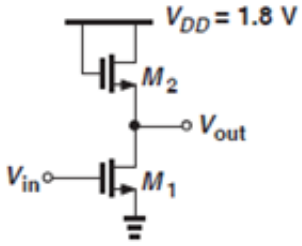


Fig. Q3 (A)

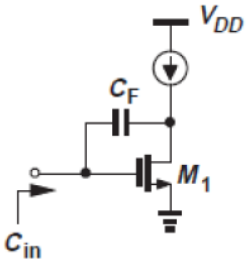


Fig. Q3 (B)

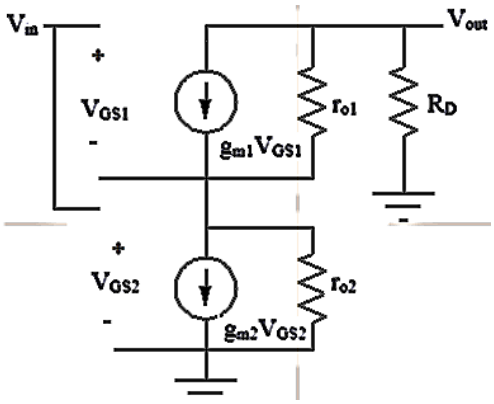


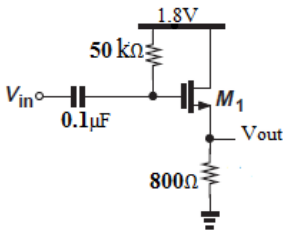
Fig. Q3 (C)

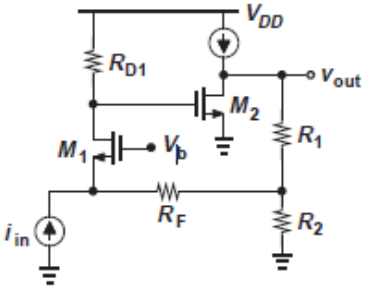
4A. Analyze the circuit shown in Fig. Q4 (A) at low and high frequencies and plot its frequency response. The circuit is connected to a load capacitance of 10pF. Assume C_{GS}=250fF, C_{GD}=80fF, C_{DB}=100fF, λ=0, V_{GS}=0.8V, V_{TH}=0.5V and $\mu_n C_{ox}$ = 100μA/V^2.

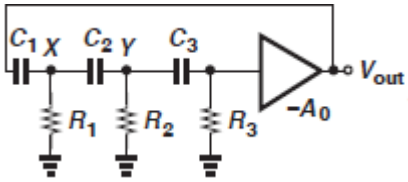
4B. Determine the closed loop gain, I/O impedances of the circuit shown in Fig. Q4 (B).

4C. Prove that negative feedback improves the bandwidth of the system.

(5+3+2)







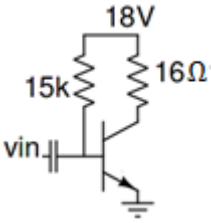


Fig.Q4 (A) **Fig.Q4 (B)** **Fig.Q5 (A)** **Fig.Q5 (C)**

5A. Determine the oscillating frequency of RC phase shift oscillator shown in Fig. Q5 (A).

5B. Determine the power efficiency of class B push pull amplifier and list its merits and demerits.

5C. For the circuit shown in Fig. Q5 (C), if the input signal has a peak current of 1 mA, determine the power efficiency. Assume β=50.

(5+3+2)