Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

THIRD SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION - NOV/DEC 2016

SUBJECT: LOGIC DESIGN (ECE - 2105)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Design a code converter that converts BCD messages into Excess 3 code. The converter has four input lines carrying signals labelled w, x, y and z, and four output lines carrying signals f_1, f_2, f_3 and f4. Implement the same using PLA.

1B. Implement 4 - to -16 decoder using two 2 - to - 4 decoders and sixteen 2-input AND gates.

1C. For the circuit given in Fig. Q1 (C) based on the input signal W, X, and Y draw the timing diagram for *V* and *Z* for the circuit. Assume that the AND gate has a delay of 10 ns and the OR gate has a delay of 5 ns.

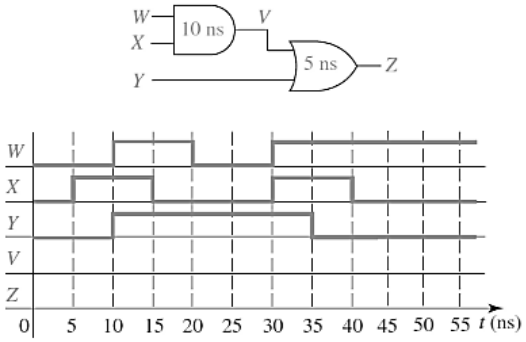

Fig. Q1(C)

(5+3+2)

2A. A switching circuit has two control inputs (C1 and C2), two data inputs (X1 and X2), and one output (Z). The circuit performs one of the logic operations OR, XOR, AND and EQU (equivalence), on the two data inputs. The function performed depends on the control inputs given in the below table. Derive the truth table for output Z. Use K-map to find the minimum AND-OR gate circuit to implement Z.

C1	C2	Function
0	0	OR
0	1	XOR
1	0	AND
1	1	EQU

2B. Design a full adder using 4 to 1 multiplexers.

2C. Show that the 2-4-2-1 code is a self-complementing code.

(5+3+2)

3A. Using the Quine-McCuskey method, determine all prime implicants of $f(A,B,C,D) = \sum m(1, 3, 5, 6, 8, 9, 12, 14, 15) + \sum d(4, 10, 13)$. Identify all essential prime implicants and find all minimum sum-of-product expressions.

3B. Design a mod-6 ripple up counter using negative edge triggered T flip-flops.

3C. Derive the characteristic equation of JK flip-flop.

(5+3+2)

4A. Design a synchronous counter which goes through the states 3,5,7 when the control signal s='0' and goes through the states 6,4,2 when control signal s='1'. Use T flip-flops.

4B. Design a 3 bit bi-directional shift register using D flip-flops.

4C. Draw the logic diagram for gated JK latch using NAND gates and write the truth table.

(5+3+2)

5A. Design an overlapping sequence detector as Moore model which detects "101" sequence in an input binary stream. Use D flip-flops.

5B. Consider an asynchronous sequential circuit with J_1=X+Y, K1=YQ and Z=QXY where X ,Y are inputs and Z is output. Write i) Next state table ii) Flow table iii) Flow diagram.

5C. Draw an ASM chart for a synchronous 2 bit up-down counter.

(5+3+2)