Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
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THIRD SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION - NOV/DEC 2016

SUBJECT: LOGIC DESIGN (ECE- 2105)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Given the Boolean expression F(A,B,C,D)=∑m(0,1,3,7,8,9,11,15).
(i) Simplify the expression using Quine Mc-Cluskey method.
(ii) Verify the same using VEM with D as the variable entering the map.

1B. Implement the function using only NOR gates F = a(b + cd)+ bc'.

1C. Define and write the formula for following gate parameters.
(i) Noise margin (ii) Propagation Delay.

(5+3+2)

2A. Consider the TABLE 2A. In the table M1M2M3M4 represents the message bits (in BCD form) and P1P2P3 represents the parity bits generated for even parity Hamming code.
(i) Complete the table.
(ii) Implement P1 using 4:1MUX with M1M2 as select inputs.
(iii) Implement P2 using two active low 3-8 decoders.
(iv) Implement P3 using suitable DEMUX.

TABLE 2A

Message bits				7 bit Hamming code						
M_1	M_2	M_3	M_4	P_1	P_2	M_1	P_3	M_2	M_3	M_4
0	0	0	0							
0	0	0	1							
0	0	1	0							
0	0	1	1							
0	1	1	0							
0	1	1	1							
1	0	0	0							
1	0	0	1							

2B. Design 2 bit comparator using 1bit comparator and necessary logic gates.

2C. Implement 3 bit Binary to Gray code convertor using PROM.

(5+3+2)

3A. A sequence detector's circuit has the following output Z and D flip-flop equations:

$D_1=Q_2X'+Q_1Q_2'X$ (MSB)

$D_2=X$

$Z=Q_1Q_2$.

Draw the state diagram of the sequence detector and also write the sequence being detected.

3B. Design an AB flip-flop using NAND gates which satisfies the truth table given in Table 3B.

TABLE 3B

A	B	OUTPUT
0	0	Q'
0	1	0
1	0	1
1	1	Q

3C. Design a 2 bit ripple up-down counter using positive edge triggered JK flip-flops.

(5+3+2)

4A. Design a Mealy type synchronous sequential circuit using D flip flop which has two inputs X_1 and X_2 which carry binary number to be added and one output which represents the sum. The inputs and outputs consist of fixed length sequences of 0's and 1's. The addition is performed serially.

4B. Design a type T self-starting counter that goes through the states 3, 4,6,7,3…

4C. Perform $745.81_{(10)} - 436.62_{(10)}$ using 9's complement method.

(5+3+2)

5A. Design a fundamental mode asynchronous sequential machine, which has two inputs x1, x2 and one output z. The initial input state is $x1 = x2 = 0$. The output value is to be 1 if and only if the input state is $x1 = x2 = 1$ and the preceding input state is $x1 = 0$, $x2 = 1$. Draw the state table, minimize and design the machine. Show all the design steps.

5B. Draw ASM chart for a synchronous decade down counter.

5C. A 3 input combinational circuit has outputs $X(A,B,C) = \sum m(1,2,4,7)$ and $Y(A,B,C) = \sum m(3,5,6,7)$. Using this circuit realize

(i) Two input OR gate (ii) Two input XNOR gate

(5+3+2)