Reg.No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

III SEMESTER B.TECH. (INFORMATION TECHNOLOGY)

MAKE UP EXAMINATIONS, NOV/DEC 2016

SUBJECT:DIGITAL SYSTEMS [ICT 2102]

REVISED CREDIT SYSTEM
(/ /2016)

Time: 3 Hours MAX.MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Design a code converter to convert a decimal digit represented in 8 4 -2 -1 to a decimal digit represented in excess -3 code, using NAND gates only. **(05)**

1B. Design an asynchronous counter using negative edge triggered JK – flip flops to generate a square waveform (with 50 % duty cycle) of frequency $\frac{1}{20}$ of input clock waveform. Also write the counting sequence. **(03)**

1C. 4 – bit carry look ahead adder is faster than 4 – bit ripple carry adder. State TRUE/FALSE. Justify. **(02)**

2A. Design a synchronous 3 bit gray code UP/DOWN counter using JK – flip flops and external gates. **(05)**

2B. Design a single digit decimal adder using 7483 ICs and external gates. **(03)**

2C. Design a 4- bit magnitude comparator using 7483 IC and NOR gates only. **(02)**

3A. Design a sequence detector with one input Y and one output Z using Moore model. The output Z is HIGH whenever the sequence "00010" is detected, otherwise the output is LOW. Overlapping of the sequence is allowed. Implement using D - flip flops and minimum number of external gates. **(05)**

3B. Design full adder/subtractor using 74153 IC and minimum number of XOR gates **(03)**

3C. Design MOD 8 ring counter using SR – flip flops. Also write all the states of the counter. **(02)**

4A. Design 2 – bit X 2 – bit binary multiplier using (i) suitable ROM (ii) PLA. **(05)**

4B. What is Race Around condition in JK – Flip Flop? With necessary diagrams, explain how master–slave JK – flip flop overcomes the same. **(03)**

4C. Design 4 to 16 line decoder using 2 to 4 line decoders only. **(02)**

5A. Simplify the given function 'F' using tabulation method. Implement the simplified expression using NOR gates only. **(05)**

$$F(A,B,C,D,E) = \sum_{m}(1,3,5,6,7,9,10,12,14,19,25,26,27) + \sum_{d}(2,8,21,22,30)$$

5B. Design SR – flip flop using NAND Latch. **(03)**

5C. Using only 7493 ICs, design a counter to count from the limits 00 to 80H continuously. **(02)**