Reg.No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

III SEMESTER B.TECH. (INFORMATION TECHNOLOGY)

END SEMESTER EXAMINATIONS, NOV/DEC 2016

SUBJECT: DIGITAL SYSTEMS [ICT 2102]

REVISED CREDIT SYSTEM
(25/11/2016)

Time: 3 Hours MAX.MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Design a 4-bit binary Carry Look Ahead adder circuit. Discuss its merits over conventional 4-bit binary ripple carry adder. **(05)**

1B. Design a 3 – bit presettable asynchronous counter using T – flip flops and using the same design a counter to count between the limits 2H to 6H. **(03)**

1C. Design a JK – flip flop using D – flip flop and external gates. **(02)**

2A. Design a synchronous UP/DOWN counter using T– flip flops and external gates to count the sequence 1 → 3 → 6 →7→2 →1 continuously. **(05)**

2B. Design a logic circuit to evaluate the arithmetic expression ($A^2 - B^2$) using 7483 IC and external gates. A and B are 3-bit binary numbers with A > B. **(03)**

2C. Design 5 to 32 line decoder using 74138 ICs and one external gate. **(02)**

3A. Simplify the given function 'F' using tabulation method. Implement the simplified expression using NAND gates only. **(05)**

$$F(A,B,C,D,E) = \sum_m (0,1,2,8,9,11,13,17,20,21,27) + \sum_d (3,5,19,22,30)$$

3B. Using 7490 IC and minimum external gates, design a sequential circuit to generate the sequence 00111011. **(03)**

3C. Design a MOD – 10 twisted ring counter using JK – flip flops. Also write all the states of the counter. **(02)**

4A. Design a code converter to convert a decimal digit represented in gray code to a decimal digit represented in 8 4 -2 -1 code, using NOR gates only. **(05)**

4B. Realize the Boolean functions **(03)**

$F_1(A,B,C) = \sum_m (0,1,3,4)$ and $F_2(A,B,C) = \prod_M (0,3,4,6)$ using suitable PLA. Also write the PLA table.

4C. Design a full subtractor using 4:1 MUXs and minimum number of external gates. **(02)**

5A. Design a sequence detector with one input Y and one output Z using Mealy model. The output Z is HIGH whenever the sequence "110111" is detected, otherwise the output is LOW. Overlapping of the sequence is allowed. Implement using T- flip flops and minimum number of external gates. **(05)**

5B. Design 2-bit magnitude comparator with cascading inputs. Using the same, design a 4 – bit magnitude comparator. **(03)**

5C. Simplify the following function into SOP and POS expressions using K – map: **(02)**

$$F(\mathrm{V}, \mathrm{W}, \mathrm{X}, \mathrm{Y}, \mathrm{Z}) = \prod_{M} (0,4,7,10,12,15,17,19,22,25) \,.\, D(1,2,6,26,30,31)$$