Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

THIRD SEMESTER B.TECH. (INSTRUMENTATION AND CONTROL ENGG.)

END SEMESTER EXAMINATIONS, DEC 2016/JAN 2017

SUBJECT: DIGITAL ELECTRONIC CIRCUITS [ICE 2103]

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. State and prove De Morgan's theorem for 2 input variables. **2**

1B. i. 425_{10} = _____ in Gray code **3**

ii. $ABC.EF_{16}$ = _____$_{10}$

iii. Find the odd one out:

a.0111 b.1000 c.1001 d.1010

1C. Using the Quine McClusky method obtain the minimal expression for the Boolean expression given by $F(A,B,C,D) = \sum m(0,1,3,5,9,10,11,13,14,15)$. **5**

2A. Design a 1 bit magnitude comparator. **2**

2B. Design and implement a 3 bit binary to gray code converter. **3**

2C. Reduce using mapping the expression $f = \pi M$ (2, 8, 9, 10, 11, 12, 14). Implement the real minimal expression using NOR logic. **5**

3A. Define the terms setup time and hold time with respect to a flip flop. **2**

3B. Realize the following function using a 4:1 multiplexer and additional gates $F(A,B,C,D) = \sum m(0,3,5,7,8,10,14)$ **3**

3C. What are the differences between a latch and a flip flop? Convert a S-R flip-flop to J-K flip-flop. **5**

4A. With a neat logic diagram, explain the working of a SISO shift register. **2**

4B. Design a synchronous 3-bit Down Counter using J-K FFs. **3**

4C. Design an overlapping sequence detector to detect the sequence 1010 using D FFs. **5**

5A. Draw the block diagram of an asynchronous sequential circuit and explain briefly. **2**

5B. Implement the full adder circuit using programmable logic array (PLA). **3**

5C. Obtain state diagram and primitive flow table for a logic system with two inputs, x and y, and one output, z, that satisfy the following conditions. Initially x=y=0, z=0. When x = 1 and y=0, then z=1. When x = 0 and y=1, z =0. The output remains in the previous state (no change) when x=y. The logic system has edge triggered inputs (no clock). **5**

****