Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

THIRD SEMESTER B.TECH. (INSTRUMENTATION AND CONTROL ENGG.)

END SEMESTER EXAMINATIONS, NOV/DEC 2016

SUBJECT: DIGITAL ELECTRONIC CIRCUITS [ICE 2103]

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A.	What are the advantages of digital systems over analog systems? What are the limitations of digital techniques?	**2**
1B.	Design a combinational circuit that accepts a 3-bit BCD number and generates an output binary number equal to the square of the input number.	**3**
1C.	Implement the function $f=[(AB)(C+D)]' + A$, using a) AOI logic b) NAND gates only c) NOR gates only.	**5**
2A.	What are alphanumeric codes? Explain different types.	**2**
2B.	Draw the truth table and obtain the logic expression of a full subtractor. Implement it using logic gates.	**3**
2C.	Design and implement a 4 bit binary to gray code converter.	**5**
3A.	Implement a 2 bit ripple counter using D flip flops.	**2**
3B.	Implement the function $F(a,b,c)=\sum m(1,3,5,6)$ using a multiplexer. Choose a and b as select inputs.	**3**
3C.	Draw the logic diagram of master slave SR flip and explain its working.	**5**
4A.	What are shift registers? Draw the schematic of a 4 bit serial in parallel out shift register using D flip flops.	**2**
4B.	Draw the logic diagram, timing diagram and truth table of a T flip flop.	**3**
4C.	Design a T counter that goes through states 0, 3, 5, 6, 0, 3 … Is the counter self-starting?	**5**
5A.	Draw the block diagram of a finite state model and explain briefly.	**2**
5B.	Implement the following Boolean functions using PAL with four inputs and 3-wide	**3**

AND-OR structure.

$F_1(A,B,C,D)=\sum m(2,12,13)$

$F_2(A,B,C,D)=\sum m(7,8,9,10,11,12,13,14,15)$

$F_3(A,B,C,D)=\sum m(0,2,3,4,5,6,7,8,10,11,15)$

5C. Obtain state diagram and primitive flow table for a logic system with two inputs, x and y, and one output, z, that satisfy the following conditions. Initially x=y=0, z=0. When x = 1 and y=0, then z=1. When x = 0 and y=1, z=0. The output remains in the previous state (no change) when x=y. The logic system has edge triggered inputs (no clock). **5**

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